ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 9, December 2013

Low Power Bist Implementation of Test Pattern Generation Based on Accumulator

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Abstract: The hardware overhead and fault coverage of a circuit is an important problem in integrated circuits and systems. To overcome this problem pseudorandom built-in-self-test (BIST) generators have been widely utilized to test integrated circuits and systems. A Pseudorandom pattern generator (PRPG) is used for generating test patterns (TPG). A weighted Pseudorandom built-in-self-test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. The test patterns are generated automatically (ATPG) for a benchmark circuit by using 3-weight pattern generator. The 3-weight WRBIST is used to reduce the test sequence lengths by improving detection probabilities of random pattern resistant faults (RPRF). So, in this part of project maximum numbers of faults are covered with automatic test pattern generation.

Keywords: ATPG - Automatic Test Pattern Generation, BIST- Built In Self-Test, RPRF- Random Pattern Resistant Fault, LT RTPG – Low transition Random Test Pattern Generation, LFSR – Linear Feedback Shift Register, WR BIST- Weighted Random

I. INTRODUCTION

Advances in VLSI technology have led to the fabrication of chips that contain a very large number of transistors. The task of testing such a chip to verify correct functionality is extremely complex and often very time consuming. In addition to the problem of testing the chips themselves, the incorporation of the chips into systems has caused test generation's cost to grow exponentially.

A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside a chip. Built-In-Self-Test (BIST) is the capability of a circuit to test itself. BIST is a design technique in which parts of a circuit are used to test the circuit itself. BIST represents a merger of the concepts of built-in test (BIT) and self-test.This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. The test patterns and the expected responses of the circuit under test (CUT) to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. Ideally, a BIST scheme should be easy to implement and must provide high fault coverage.

A. Bist Techniques

BIST techniques can be classified into two categories, namely **on-line BIST**, which includes concurrent and non-concurrent techniques, and **off-line BIST**, which includes functional and structural approaches.

B. Test Pattern Generation of Bist

Test pattern generation is the process of defining an effective test set which will drive the circuit under test so that the faults in the circuit. The algorithm used in test pattern generation are usually directed to non-functional testing, which concentrate on propagating any available faults on the circuit nodes to primary outputs. This type of testing is termed fault oriented testing. Test pattern generation is strongly related to fault modelling.

Test pattern generation approaches for BIST schemes can be divided into four categories:

1. Exhaustive testing
2. Pseudorandom testing
    a. Weighted test generator
    b. Adaptive test generator
3. Pseudoexhaustive testing
4. Deterministic testing

II. EXISTING SYSTEM

A. Accumulator cell Design

An Accumulator Cell is designed with Full adder and D-flip flop with set and reset inputs. According to these schemes a typical weight assignment procedure would involve separating the test set into two subsets as follows S1 = {T1,T4} and S2 = {T2,T3}, The weight assignments for these subset is W(S1)={-,-,1,-,1} and W(S2)={-,-,0,1,0}, where a "-" denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0" indicates

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ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 9, December 2013

that the input is driven by the logic "0" value. The implementation of the weighted-pattern generation scheme is based on the full adder truth table.

1. Operation of Accumulator cell:

A fig 1 shows an accumulator cell with full adder and D-flip flop. In this the upper D-flip flop uses set as reset and reset as set inputs. The output of upper D-flip flop is given as input of full adder. The output of full adder is connected with another d-flip flop with actual set and reset inputs. Full adder uses 3 inputs, 2 inputs from output of both D-flip flops, and another input is Cin. The sum output of full adder is given as input of D-flip flop.

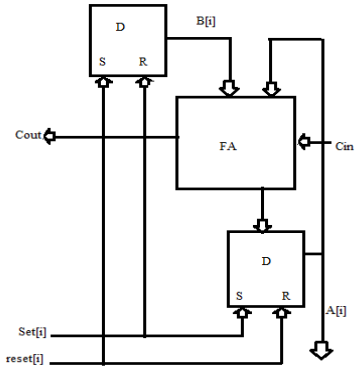

Fig. 1 Accumulator cell

2. Configuration of Accumulator cell:

There are three configurations for Accumulator cell is proposed. It is shown in Fig 2.The configuration (a) in Fig 2 that drives the CUT inputs when A='1' is required. Set[i] = '1' and reset[i] ='0' and hence A='1' and B='0'. Then the output is equal to '1', and Cin is transferred to Cout.

The configuration (b) that drives the CUT inputs when A='0' is required. Set[i] = '0' and reset[i]='1' and hence A='0' and B='1'. Then the output is equal to '0', and Cin is transferred to Cout.

The configuration (c) that drives the CUT inputs when A='-' is required. Set[i]='0' and reset[i]='0'.

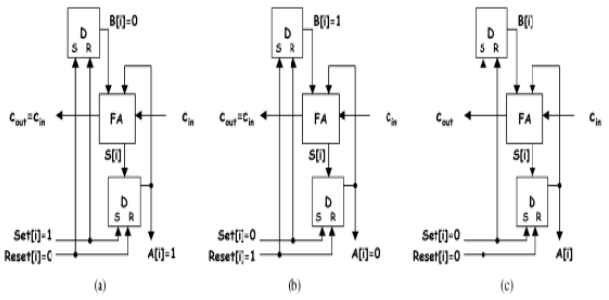

Fig. 2 Configurations of accumulator cell

This condition is also referred as 0.5 weight output or don't care state. The D input of the flip flop of the register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate random patterns to the inputs of the CUT.

B. Testing a Circuit By Using Test Vectors

A fig 3 shows a C17 benchmark circuit. In this 5 inputs are used.

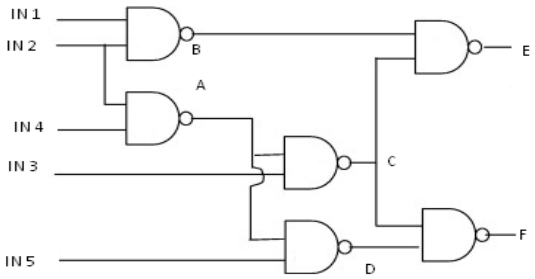

Fig. 3 C17 Benchmark circuit

The weights are applied through set and reset values, the test vectors are generated automatically by pseudorandom method. The fault coverage is calculated. Fig 4 show a C17 benchmark circuit with inputs from accumulator cell output.

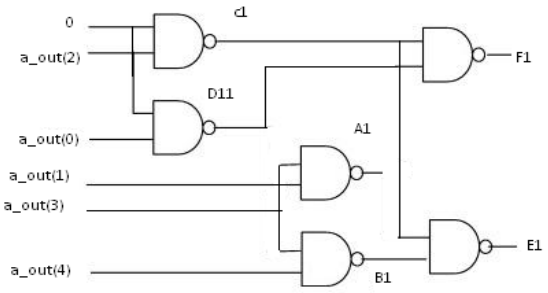

Fig. 4 C17 Benchmark circuit with inputs from accumulator cell output

A benchmark circuit is taken and it is tested by using test vectors which is generated by using pseudorandom pattern generation method. A C17 benchmark circuit is taken and tested by using test vectors. The fault coverage is more by applying these test vectors. These outputs are used as inputs for another benchmark circuit. Stuck-at-fault is applied and test vectors are generated automatically

The output of accumulator cell are a_out(0),a_out(1),a_out(2),a_out(3),a_out(4). These outputs are used as inputs for another benchmark circuit. Stuck-at-fault is applied and test vectors are generated automatically. The faults are covered by test vectors. The fault coverage is more by applying these test vectors.

If the fault output is '1' means, it indicates that **"fault is detected"**. If the fault output is '0' means, it

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 1, Issue 9, December 2013

indicates that**, "fault is not detected"**. Mostly 90% of faults are detected so, the fault coverage is more.

III. PROPOSED DESIGN

A. LOW POWER BIST

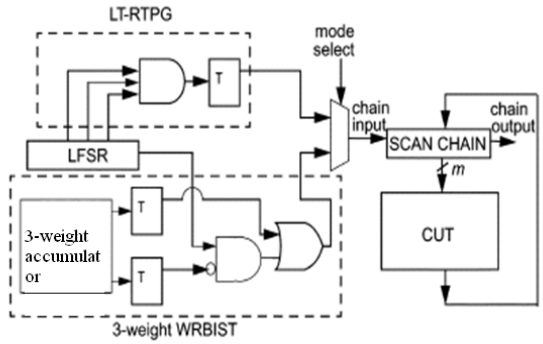

Fig. 5 Architecture of LOW POWER BIST

The proposed Low Power BIST is comprised of two TPGs: an LT-RTPG and a 3-weight WRBIST is shown in Fig 5. Built-in Self Test (BIST) is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

The multiplexer, which drives the input of scan chain, selects a test pattern source between the LT-RTPG and the 3-weight WRBIST. In this, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults. In next technique, test patterns that are generated by the 3-weight WRBIST are selected to detect the faults that remain undetected after the first session.

1. LT-RTPG BIST

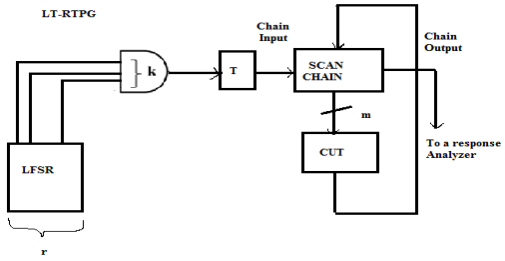

Fig 6 Architecture of LT-RTPG

Excessive switching activity during test application can damage CUTs during BIST. The LT-RTPG reduces switching activity during BIST by reducing transition at scan inputs during scan shift operations. This implies that RPRFs that escape LT-RTPG test sequences can be effectively detected by fixing selected inputs to binary values specified in deterministic test cubes for these RPRFs and applying random patterns to the rest of inputs. This technique is used in the 3-weight WRBIST to achieve high fault coverage for random pattern resistant circuits.

2. WR-BIST

In the 3-weight WRBIST scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs; the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF. The Architecture of WR-BIST is shown in Fig 7.

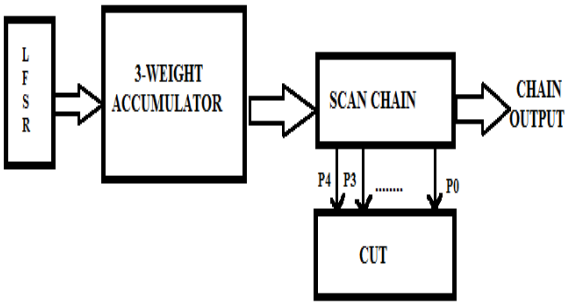

Fig 7 Architecture of WR-BIST

IV. SIMULATION RESULTS

A. Simulation Result for Accumulator cell Configurations

The waveform of Accumulator cell's configurations is shown in the fig 8. The configuration (a) that drives the CUT inputs when A='1' is required. Set[i] = '1' and reset[i] ='0' and hence A='1' and B='0'. Then the output is equal to '1', and Cin is transferred to Cout.

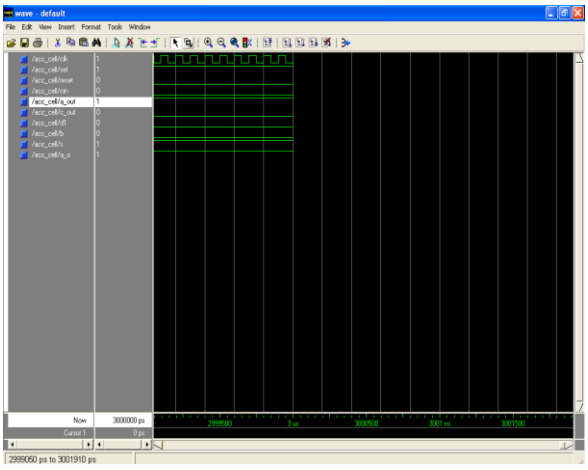

Fig 8. Waveform for the configuration of set='1' and reset='0'

The waveform for Accumulator cell with set='0' and reset='1' is shown in the Fig. 9.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

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INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
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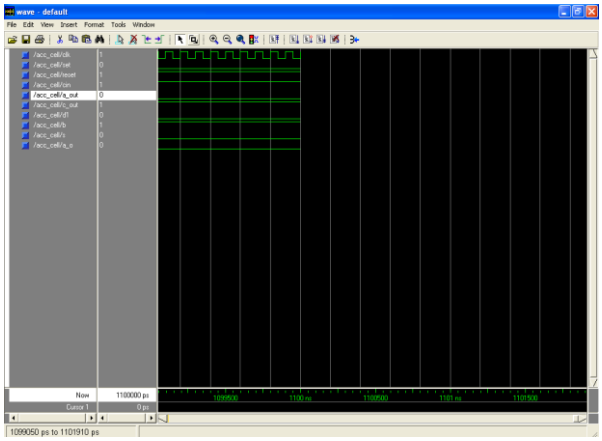

Fig. 9 waveform of the configuration of set='0' and reset='1'

The waveform for Accumulator cell with set='0' and reset='0' is given in fig 10.

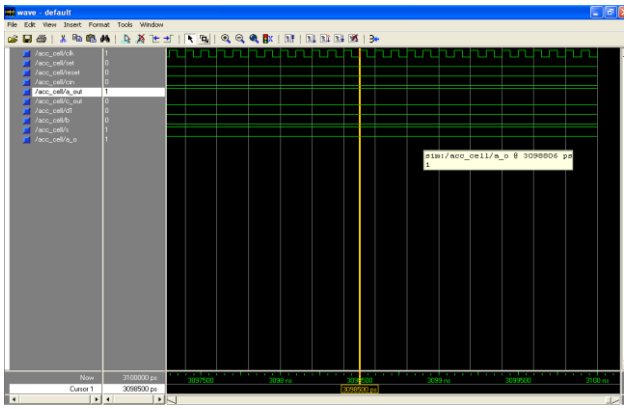

Fig. 10 Waveform of the configuration of set='0' and reset='0'

1. Simulation Result for Test Vector Generation for Fault Coverage:

Fig 11 shows the applied test vectors for set and reset are "10000" and "10001" respectively. If fault is present means fault output parameter is set as'1'. If no fault in circuit means, fault will be set as '0'. For this applied test vectors the test patterns are generated automatically.

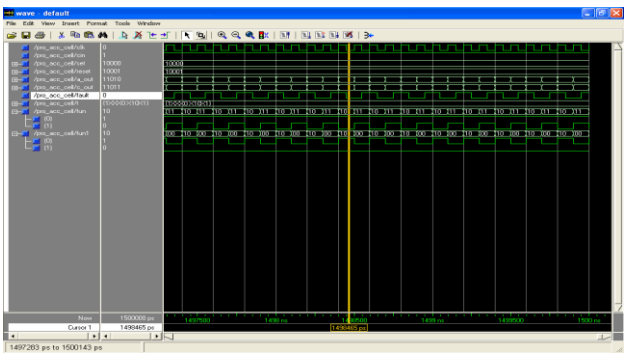

Fig. 11 Output Waveform For Benchmark Circuit Using Accumulator Cell

2. Simulation Result for LT-RTPG

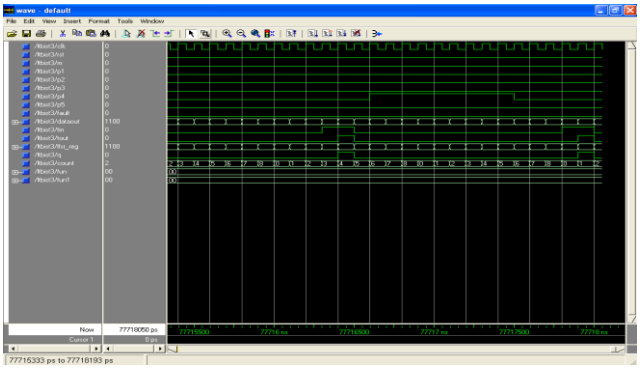

Fig. 12 Output Waveform of LT-RTPG for Fault not detected

Fig 12 shows the output waveform for LT-RTPG. It is the waveform for fault not detected because the fault is shown as '0'.

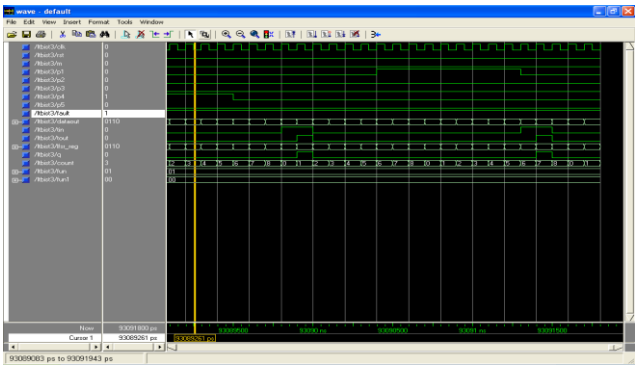

Fig 13 Output waveform for LT-RTPG for Fault detected

3. Simulation result for WR-BIST

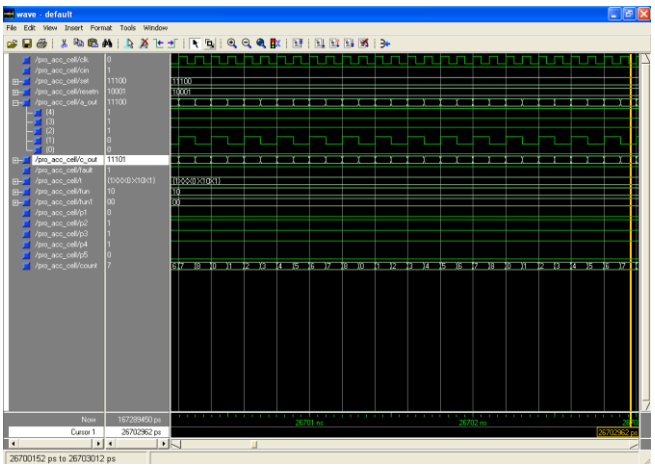

Fig 14 Waveform of WR-BIST with high fault coverage

In Fig 14 clk , Cin, set and reset are the inputs. C_out , fault, p1,p2,p3,p4,p5 are the outputs. Set and reset values for generated patterns are "11100" and "10001"… fault coverage for this vector is 100%.

4. Simulation Result for LOW-POWER BIST

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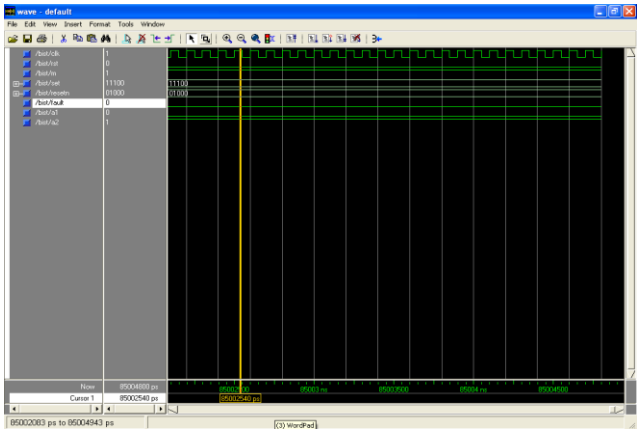

Fig 15 Waveform of LOW-POWER BIST for fault not detected

Fig 15 shows the waveform of Low0Power BIST for fault not detected. In this clk, rst , and m are the inputs of the Low-Power BIST. f1,f2 are the outputs of the Low-Power BIST.

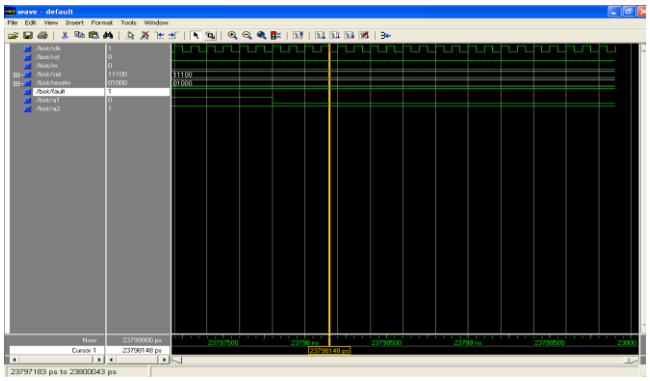

Fig 16 Waveform of LOW-POWER BIST for fault detected

Fig 16 shows the waveform of Low0Power BIST for fault detected. In this clk, rst , and m are the inputs of the Low-Power BIST. f1,f2 are the outputs of the Low-Power BIST.

V. POWER TABLE

TABLE I
POWER AND FAULT CALCULATION

Series	Accumulator	Low-Transition BIST	Weighted Random BIST	LOW-POWER BIST
power[w]	0.08	0.025	0.024	0.020
Fault coverage[%]	50	75	90	100

A. Power and Fault Comparison Chart

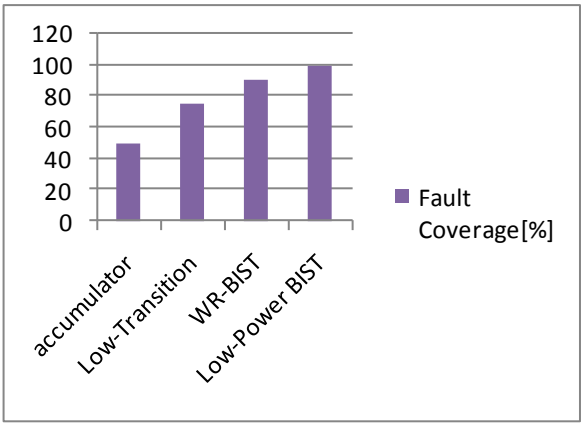

Fig 17 Fault Comparison Chart

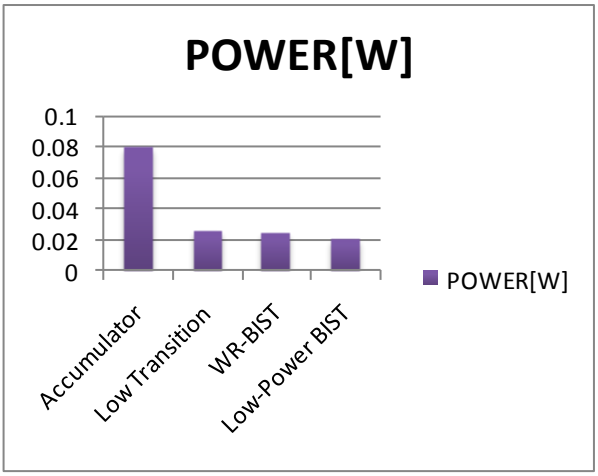

Fig 18 Power Comparison Chart

VI. CONCLUSION

This project presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with an arguable length of test sequence. The test patterns are engender by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs) only with (pseudo) random patterns generated by an LFSR often require unforeseeable long test Sequences thereby resulting in prohibitively long test time. The proposed TPG LT-RTPG and 3-weight WRBIST reduces switching activities in the circuits, so that the number of transitions will be debase an d less power will be consume.

ACKNOWLEDGEMENT

We thank to Dr.S.V.Saravanan, Christ The King Engineering College, Coimbatore, for their contribution of this work.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
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