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AN EFFICIENT CLOSED LOOP CONTROLLED BRIDGELESS CUK RECTIFIER FOR PFC APPLICATIONS

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Abstract: This paper presents the digital simulation of single phase AC-DC Bridgeless Cuk for Power Factor Correction (PFC) rectifiers. A conventional Cuk PFC rectifier suffers from high conduction losses due to presence of input rectifier bridges. Higher efficiency can be achieved by using the bridgeless Cuk topology. The conduction losses are considerably reduced due to the absence of input diode bridge and availability of only two semiconductor devices in the current flowing path during each switching cycle. By operating the improved topology in discontinuous conduction mode (DCM), it ensures unity power factor and low total harmonic distortion (THD). A closed loop controlled bridgeless Cuk PFC converter is modelled and simulated.

Keywords: Bridgeless rectifier, Cuk topology, Discontinuous Conduction Mode (DCM), low conduction losses, Power Factor Correction (PFC) rectifier, total harmonic distortion(THD).

I. INTRODUCTION

In recent years, there have been enhancing demand for improving power quality of ac system due to the increased numbers of power electronic equipment. Presently, there exists an immense demand for high power factor and low total harmonic distortion in the input current. With the rigorous requirements of power quality, power factor correction (PFC) rectifiers are becoming very necessary and considerable research efforts have been directed towards the development of PFC converters. As a matter of fact, the PFC circuits are becoming mandatory as more rigorous harmonic regulations and standards such as IEC 61000-3-2 on total harmonic distortion of input current are imposed.

The active PFC is the most desirable type of power factor correction (PFC) circuits, as it makes the load behave like a pure resistor to attain almost unity power factor and negligible harmonics in the input current. Most of the active PFC circuits comprise a front end bridge rectifier followed by dc-dc converter. During each switching cycle, the power flows through atleast three semiconductor devices including two rectifier diodes and one switch. As a result, significant conduction loss across bridge diode begins to degrade the overall system efficiency.

Recently, in an effort to improve the efficiency, several researchers have started looking into bridgeless PFC circuit topologies. A bridgeless PFC circuit allows current to flow through less number of switching devices. Accordingly, conduction losses are considerably reduced and higher efficiency can be obtained.

Most of the presented bridgeless topologies so far implement boost type due to its simplicity and low cost. The main limitation with this topology is high start-up inrush current and dc output voltage is higher than the peak input voltage. To overcome these drawbacks, various topologies have been introduced in this regard. However, buck converter results in reduced power factor and enhanced THD.

In this paper, the modelling and simulation of bridgeless Cuk PFC rectifier is presented. Performance comparison between conventional and proposed bridgeless Cuk PFC rectifier are performed based on simulation results.

II. BRIDGELESS CUK PFC RECTIFIERS

The circuit configuration of bridgeless PFC circuits based on Cuk topology with low conduction losses is shown in Fig.1. Unlike boost converter, the Cuk converter offers several desirable features such as easy implementation of transformer isolation, natural protection against inrush current, lower current ripple, less electromagnetic interference (EMI) associated with the DCM topology and has continuous input and output currents with low current ripple.

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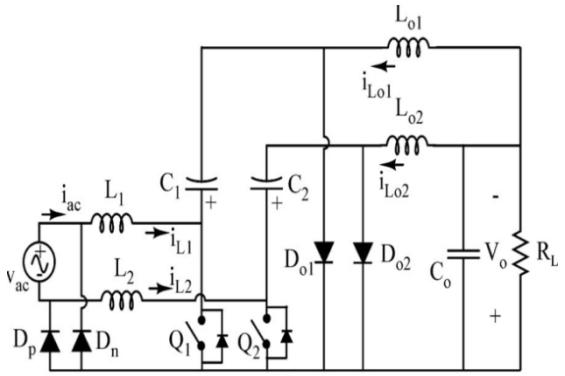


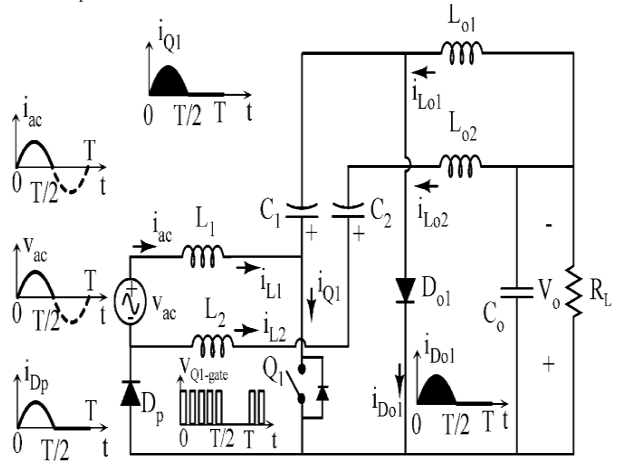
Fig. 1. Bridgeless Cuk PFC rectifier

The bridgeless topology of Fig.1 are formed by connecting two dc-dc Cuk converters, one for positive half-line period and other for negative half-line period of the input voltage. The bridgeless topology utilizes two power switches Q1 and Q2, driven by same control signal which simplifies the control circuitry. Dp and Dn are slow recovery diodes. The output diodes are Do1 and Do2. L1 and L2 are input inductors. The output inductors are Lo1 and Lo2.The capacitors C1 and C2 are the medium for transferring energy from source to load. The filter capacitor Co is made large enough to reduce output ripple.

By referring Fig.1, during positive and negative half line period, the current flows through one or two semiconductor devices. Therefore, current stresses are greatly reduced and circuit efficiency is further improved compared to the conventional Cuk rectifier. Moreover, Fig.1 shows that one rail of output voltage is always connected to the input ac line through slow recovery diodes D_p and D_n. Thus, the bridgeless topologies do not suffer from EMI problem. Consequently, the bridgeless topologies appear to be excellent choice for commercial PFC products.

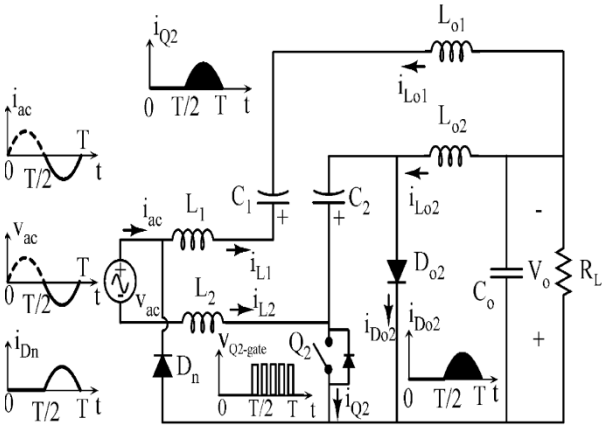
III. PRINCIPLE OF OPERATION OF THE BRIDGELESS PFC RECTIFIER

The bridgeless rectifiers shown in Fig.1 are constructed by connecting two dc-dc converters. Referring to Fig 2.(a) during the positive half-line cycle, the first dc-dc Cuk circuit, L_1- Q_1 - C_1 - L_{o1} - D_{o1} , is active through diode D_p ,which connects the input ac source to the output.



(a) During positive half-line period

During the negative half-line cycle, as shown in Fig 2.(b), the second dc-dc Cuk circuit, L_2 -Q_2 -C_2-L_{o2}-D_{o2} is active through diode D_n ,which connects the input ac source to the output.



(b) During negative half-line period

Fig. 2. Equivalent circuits for bridgeless Cuk PFC rectifier

The operation of the converter is symmetrical in two half cycles of the input voltage. Therefore it is sufficient to explain the converter operation during positive half cycle of the input voltage. By operating the rectifier in DCM, several advantages can be attained. These advantages include inherent unity power factor, low total harmonic distortion. It provides additional advantages such as zero current turn-ON in the power switches, zero current turn-OFF in the output diodes and simple control circuitry. Thus, switching losses and reverse recovery of output diodes are greatly reduced. The average voltage across capacitor C_1 during the line cycle can be expressed as follows.

$$v_{c1}(t) = \begin{cases} v_{ac}(t) + V_o\ ,\ 0 \le t \le \frac{T}{2} \\ V_o,\ \frac{T}{2} \le t \le T \end{cases} \qquad (1)$$

where T represents the period of the line voltage.

IV. MODES OF OPERATION

The circuit operation can be partitioned into three different operating modes during one switching period T_s in a positive half-line period. Equivalent circuits over a switching period T_s in the positive half-line period is shown in Fig 2. (a). The modes of operation over a switching cycle can be briefly described as follows.

Mode 1[t_o, t_1]

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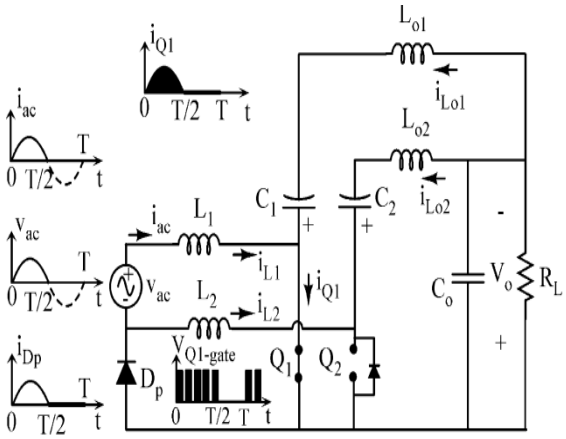

Fig. 3. Topological mode - when switch Q1 is ON

This mode begins when the switch Q_1 is turned ON. Diode D_p is forward biased by the inductor current i_{L1}. As a result, the diode D_n is reverse biased by the input voltage. The output diode D_{o1} is reverse biased by the reverse voltage (v_{ac} + V_o), while D_{o2} is reverse biased by the output voltage.

In this mode, the currents through inductors L_1 and L_{o1} increase linearly with the input voltage, while the current through L_{o2} is zero due to the constant voltage across C_2.

Mode 2 [t_1, t_2]

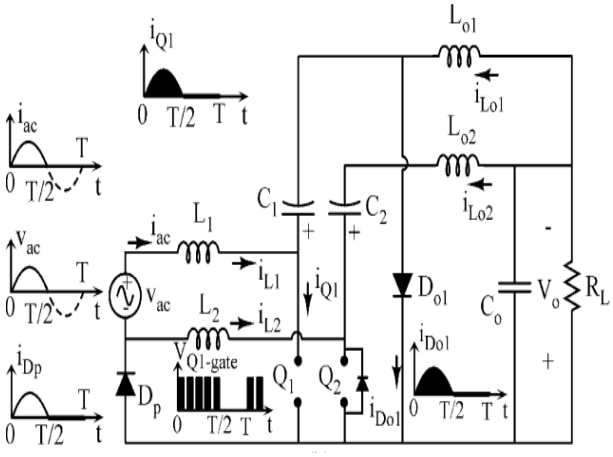

Fig.4.Topological mode - when switch Q1 is OFF

This mode begins when the switch Q_1 is turned OFF and the diode D_{o1} is turned ON simultaneously providing a path for the inductor currents i_{L1} and i_{Lo1}. The diode D_p remains conducting to provide a path for i_{L1}. Diode D_{o2} remains reverse biased during the interval. This interval ends when i_{Do1} reaches to zero and D_{o1} becomes reverse biased. Note that the diode D_{o1} is switched OFF at zero current.

Mode 3 [t_2, t_3]

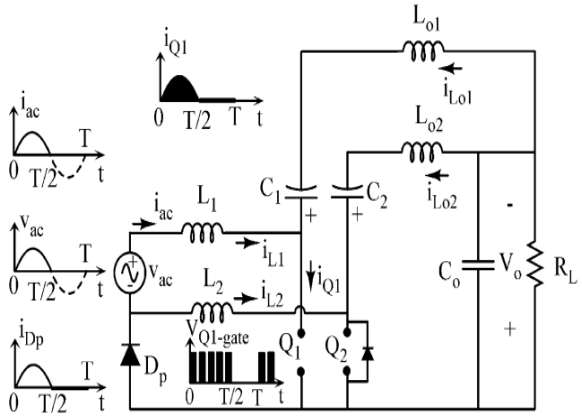

Fig.5. Topological mode – In DCM topology

During this interval, only the diode D_p conducts to provide a path for i_{L1}. Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor C_1 is being charged by the inductor current i_{L1}. This period ends when Q_1 is turned ON.

V.COMPARISON BETWEEN CONVENTIONAL AND BRIDGELESS CUK PFC RECTIFIER

The bridgeless Cuk PFC rectifier is compared to the conventional Cuk PFC with respect to their component count, THD and efficiency. The bridgeless Cuk is constructed by connecting two dc-dc Cuk converters, one for each half line period, which allows current to flow through two semiconductor devices. Hence the current stresses in the switches are reduced. Accordingly, the converter conduction losses are greatly reduced and efficiency is further improved compared to the conventional rectifier. The comparison between the conventional and the bridgeless Cuk PFC rectifier as shown in Table1 is done based on simulation results. Furthermore, Matlab Simulink is used to simulate the circuit. The converters were simulated for an output voltage of 48V under input voltage of 100 Vrms.

Table .1 Comparison between Conventional and bridgeless Cuk PFC rectifier

Item	Conventional Cuk PFC	Bridgeless Cuk PFC
Slow Diode	4	2
Fast Diode	1	2
Switch	1	2

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Current conduction path	SW ON	2 slow diodes and 1 switch	1slow diode and 1 switch
	SW OFF	2 slow diodes and 1 fast diode	1slow diode and 1fast diode
	DCM	2 slow diodes	1slow diode

VI. SIMULATION RESULTS

The simulation is carried out using Matlab Simulink for the following data specifications:
V_{ac} = 100V_{rms}, V_o = 48V, f_{sw} =100kHz, f_s =50Hz and the results are presented . The simulation result discusses the conventional Cuk PFC rectifier and then the bridgeless Cuk PFC rectifier in open loop model and finally the bridgeless Cuk PFC rectifier in closed loop model. The conventional Cuk PFC converter is shown in Fig 6.a.The corresponding AC input voltage and current waveforms are shown in Fig.6.b.

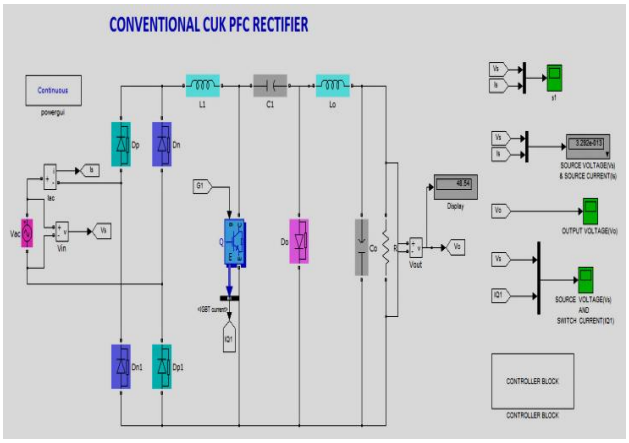

Fig 6. (a) Conventional Cuk PFC rectifier

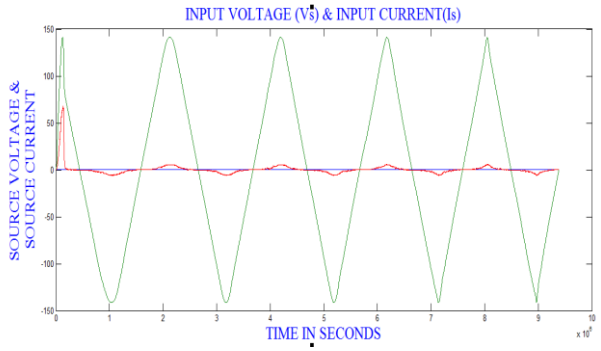

Fig 6.(b) AC input Voltage and current

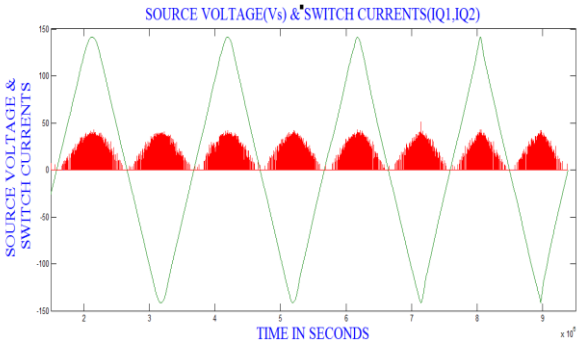

Fig 6.(c) AC input Voltage and Switch current (IQ)

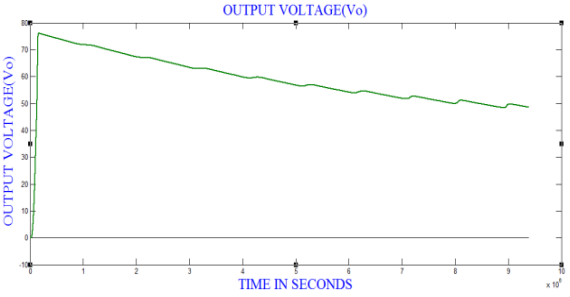

Fig 6.(d) DC Output Voltage

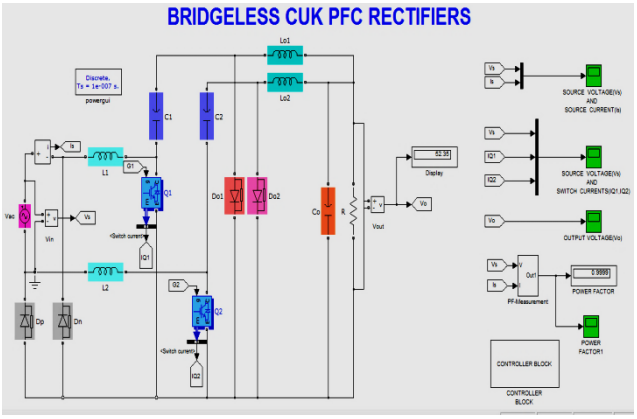

Fig 7. (a) Open loop controlled Cuk converter

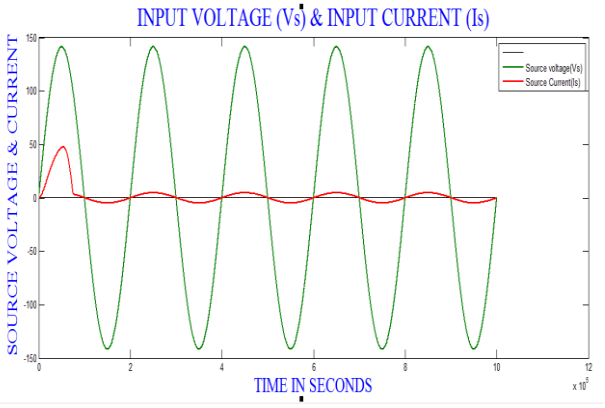

Fig 7.(b) AC input Voltage and current

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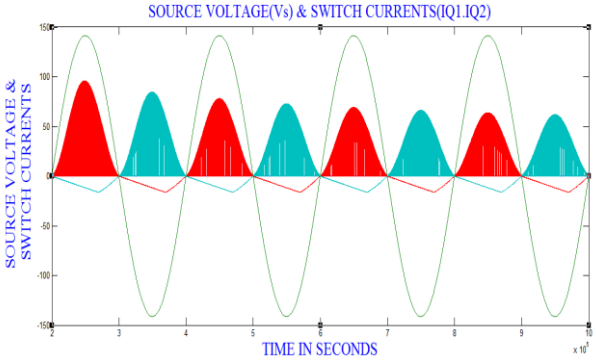

Fig 7.(c) AC input Voltage and Switch currents (IQ1, IQ2)

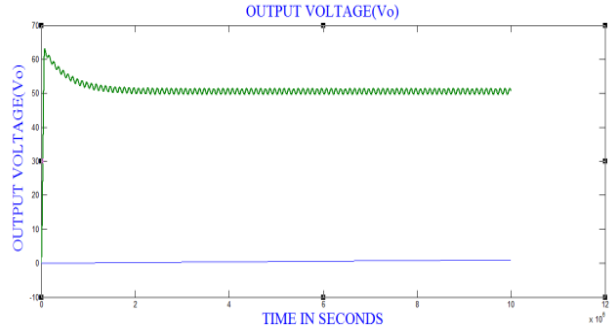

Fig 7.(d) DC Output Voltage

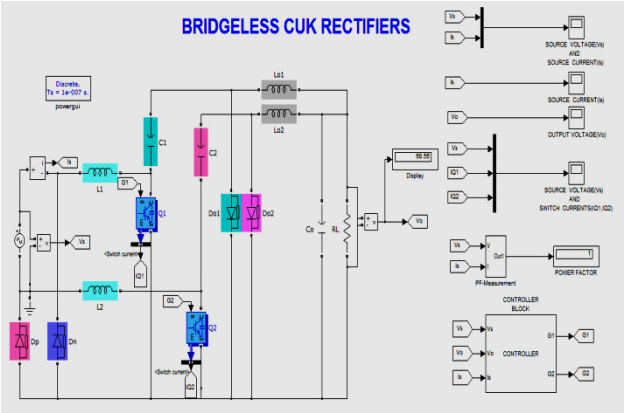

Fig 8. (a) Closed loop controlled Cuk converter

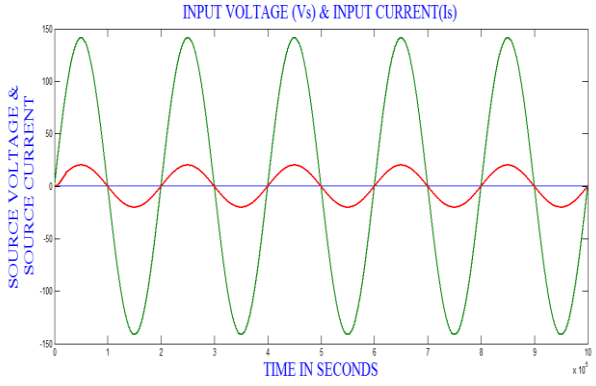

Fig 8.(b) AC input Voltage and current

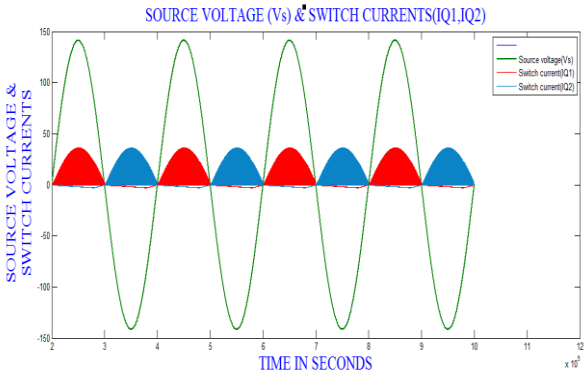

Fig 8.(c) AC input Voltage and Switch currents (IQ1, IQ2)

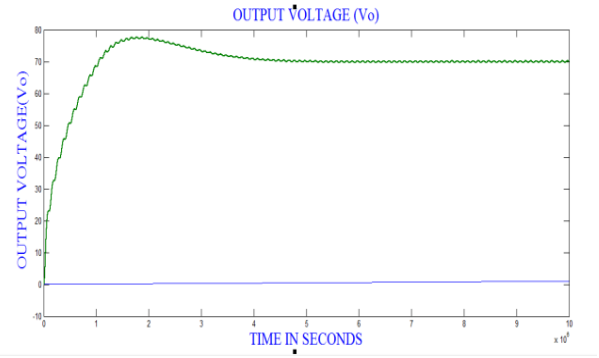

Fig 8.(d) DC Output Voltage

Open loop controlled Cuk converter circuit is shown in Fig 7.a.DC output voltage of 48V is shown in Fig 7.d. Closed loop system is shown in Fig 8.a. Output voltage is sensed and it is compared with a reference voltage. The error is processed through a PI controller. The output of the pulse generator controls the output voltage till it reaches the set value. It can be seen that the DC voltage reaches the set value as shown in Fig 8.d.

VII. CONCLUSION

A single phase ac-dc bridgeless Cuk PFC rectifier with low conduction losses and low input current distortion is modelled and simulated using MATLAB Simulink. Open loop and closed loop models are developed and they are used successfully for simulation. The capability of this topology is verified via simulation results. The simulation studies indicate that the power factor is nearly unity and obtained low THD by employing Cuk converter. Due to the lower conduction and switching losses, the proposed topologies can further improve the conversion efficiency when compared with the conventional Cuk PFC rectifier. The proposed circuit meets IEC-1000-3-2 requirements. The simulation results are in line with prediction. This work has covered the simulation of open loop and closed loop controlled PFC converter.

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BIOGRAPHIES

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