

# A New Strategy of Series-Shunt Power Quality Compensator

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**Abstract:** Every new technology evolved with minimalism as well as stumbling blocks, as the recent innovations and excessive use of power electronic devices such as, fast switching uncontrolled/controlled converters, invertors and cyclo-converters, high voltage power converters used in HVDC etc. make the system flexible to work but also a complex problem of power quality has evolved, the measure of it was voltage and current harmonics, low power factor, reactive power demand etc. Ideally power system network must be electrically clean, harmonics free, balanced, regulated voltage at point of common coupling and must have a unity power factor. In this paper, the analysis of the Series-Shunt Power Quality Compensator (S-SPQC) is presented for three-phase three wire distorted system conditions, in this topology two types of active filter i.e. Series (SAF) and Parallel (PAF) are integrated to accomplish the goal of improving voltage quality by SAF and current quality by PAF. In combined approach of S-SPQC, SAF part is designed by using Synchronous Reference Frame (SRF) technique while PAF part is designed by using Indirect Current Control (ICC) technique. The MATLAB/ Simulink based simulation results are graphically shown as well as tabulated in detail which reflects the performance of the S-SPQC control method discussed in this paper.

**Keywords:** Power Quality, Harmonics, Direct and Quadrature Axes, Series-Shunt Power Quality Compensator (S-SPQC), Voltage Reference Generation, Current Reference Generation

## I. INTRODUCTION

With day to day advancement in the world, electricity is becoming the primary need to everyone. It is important to provide a clean & good quality power to the consumers as well as to maintain it at the PCC. There is a boom in the development of the power electronic devices which drops the quality of power at the PCC, which has adverse effects on the power system. To avoid such problems there is a vast research on power filters is going on continuously.

Recently advanced active power filtering techniques identifies superiority than passive filters because of the performance, compactness and response to eliminate harmonics and compensate burden of reactive power generated by the nonlinear loads [1]. Now a days, by combining the series and shunt converters having a common capacitive storage device, it is possible to overcome nearly all kind of power quality problems which is known as Series Shunt Power Quality Compensator (S-SPQC) [2]. The function of S-SPQC system is to compensate problems associated with the voltage and current profiles, which ideally have harmonic free Voltage and current waveforms, unity power factor of load, balanced load, stabilized/ regulated voltage across dc link capacitor, negligible reactive power demand and maintain constant voltage at point of common coupling (PCC) under load variation and fault condition. The current related compensation is provided through PAF connected near the loads and the voltage related compensation is provided through SAF connected in series with a line through a

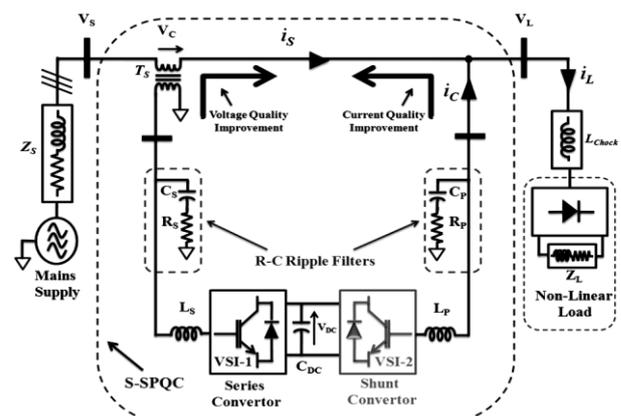


Figure 1. Schematic diagram of S-SPQC

series transformer and functions as a controlled voltage source [2-5].

There are so many controlling techniques presented in the various literatures out of that, SRF technique consisting of phase locked loops [5,6,8] and ICC technique consisting of Source Current tracking system [11,12] so there is not much effect of voltage distortion and these techniques found to be very simple to design, requires less number of sensors and fast responding. SRF technique uses Clark's and Park's Transformation for voltage reference generation. ICC technique which need not require load and filter current measurements, works on direct axis and quadrature axis component using unit templates for current reference

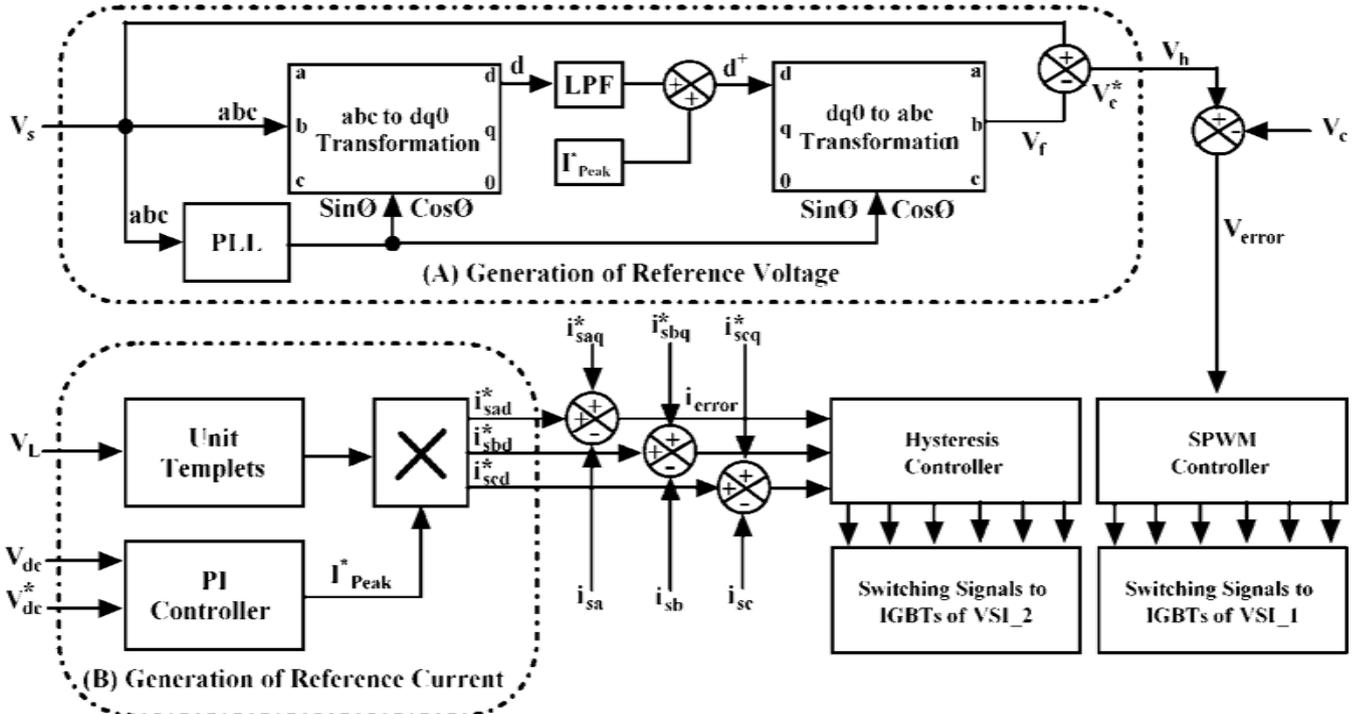


Figure 2. Proposed S-SPQC control algorithm block diagram (A) Generation of reference voltage (B) Generation of reference current

generation. Considering quadrature axis component system provides voltage regulation if required otherwise maintains load unity power factor, due to which system performance is improved.

In this paper a new control algorithm by integrating the SRF and ICC techniques for the Series-Shunt Power Quality Compensator (S-SPQC) is presented. MATLAB/Simulink software based Simulation is carried out and results are mentioned, which shows the usefulness of the control algorithm.

converters. S-SPQC has the capability to compensate voltage and current related problems like harmonics compensation, voltage flickers, imbalance, regulation and power factor improvement, neutral current control, reactive power compensation, dc-link voltage stabilization and load unbalance minimization.

#### A. Series APF

1) *Generation of reference voltage by SRF technique:* Voltage perturbations like sag, swell, flicker & harmonics in the source side mainly compensated using series APF, caused by the faults in the distribution line or sudden rise in the load at the PCC. The reference voltage value which is nothing but the harmonic component of the voltage is calculated by SRF technique shown in Fig. 2(A). After comparing the harmonic component  $V_h$  with AC side filter component  $V_c$  the error signal  $V_{error}$  is fed to sinusoidal PWM controller [6-8].

In equation (1), supply voltages  $V_s$  are transformed from a-b-c to d-q-0 coordinates [5,6].

In equation (2), the direct axes voltage ( $V_{sd}$ ) contains a DC (average  $\bar{V}_{sd}$ ) and AC (oscillating  $\tilde{V}_{sd}$ ) components of

## II. S-SPQC CONTROL ALGORITHM

The S-SPQC is mainly a combination of series and shunt active filters with a commonly shared DC link. In SAF series converter operates as voltage source inverter, while in PAF inverter operates as a current source. Fig. 1 describes the basic blocks of the S-SPQC consisting of series and shunt

source voltages from that,  $\bar{V}_{sd}$  is separate out by using low pass filter.

The estimated amplitude of the source current  $I_{Peak}^*$  added up with the average voltage component  $\bar{V}_{sd}$  in order to maintain the DC link capacitor voltage at specified value. Then, the total average voltage component  $\bar{V}_{sd}^+$  will be as given in equation (3).

The fundamental components of voltages  $V_f$  are calculated by transforming d-q-0 axis voltages to a-b-c coordinates, as given in equation (4).

$$\begin{bmatrix} V_{s0} \\ V_{sd} \\ V_{sq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (1)$$

$$V_{sd} = \bar{V}_{sd} + \tilde{V}_{sd} \quad (2)$$

$$\bar{V}_{sd}^+ = \bar{V}_{sd} + I_{Peak}^* \quad (3)$$

$$\begin{bmatrix} V_{fa} \\ V_{fb} \\ V_{fc} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) & 1 \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} \bar{V}_{sd}^+ \\ 0 \\ 0 \end{bmatrix} \quad (4)$$

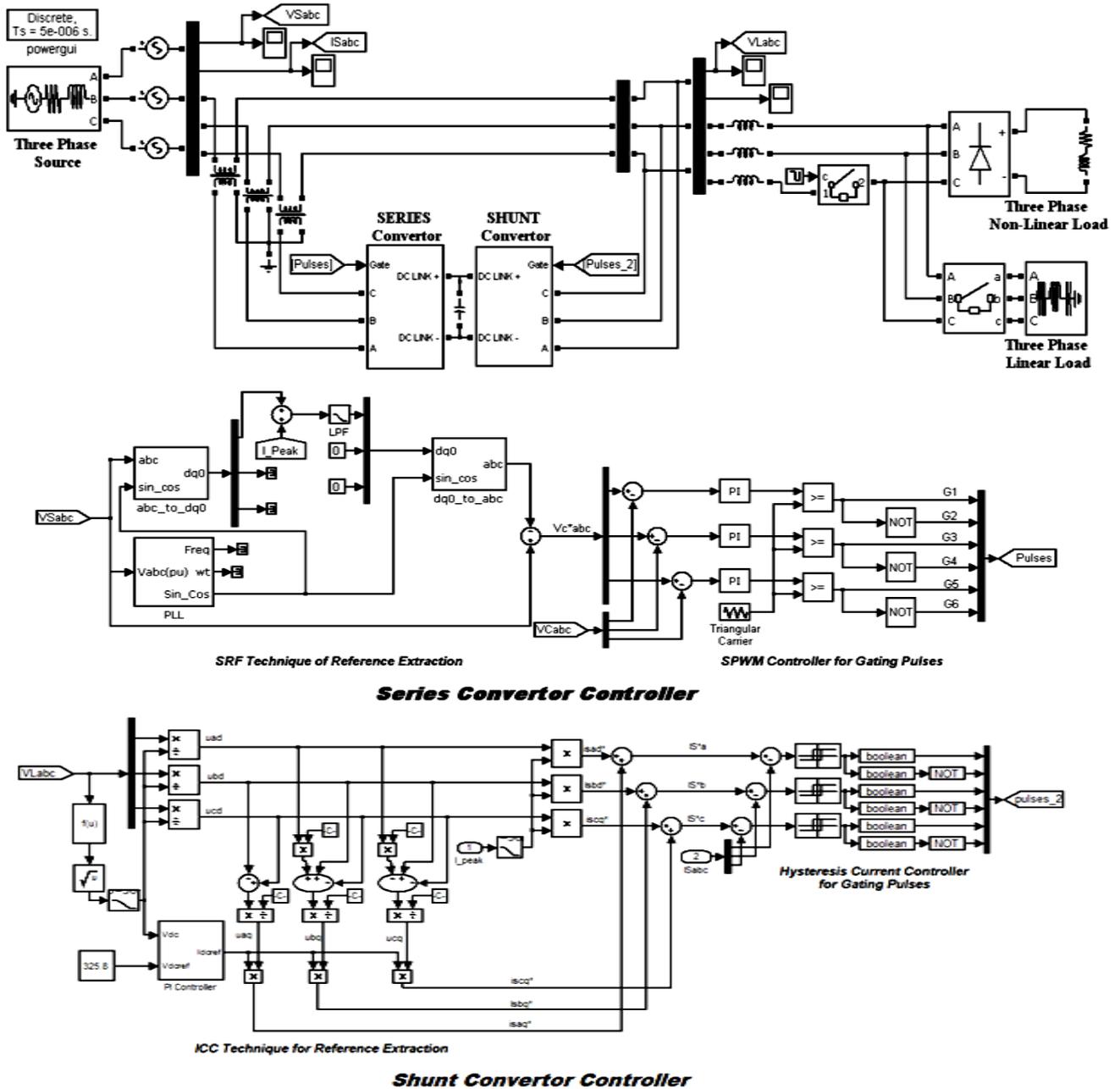


Figure 3. MATLAB Model of Proposed S-SPQC scheme

This fundamental component is then subtracted from source voltage  $V_s$  to get harmonic reference compensating component  $V_C^*$ . The switching signals are then generated for series converter IGBT switches by comparing reference compensating component voltages ( $V_C^*$ ) and the actual filter voltages ( $V_C$ ) and processing the error signal  $V_{error}$  via sinusoidal PWM controller.

2) *SPWM Controller*: In this controller high triangular carrier frequency (5 kHz) is compared with low frequency signal shown in Fig. 3. PI controller is used to control the low frequency error signal  $V_{error}$  within a given limiter range, then the controlling signal is compared with a carrier signal resulting in the switching signals to the gates.

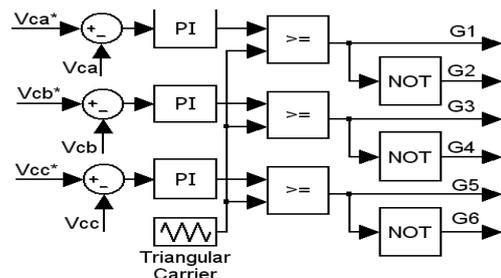


Figure 4. Sinusoidal PWM controller

### B. Shunt APF

1) *Generation of reference current by ICC technique*: Fig. 2(B) shows the ICC Algorithm of the S-SPQC [9]. The control scheme of the S-SPQC requires sensing of

voltages  $V_L$  at PCC and dc bus voltage  $v_{dc}$ . A dc bus capacitor balancing is achieved by adjusting the Proportional and Integral gain of the PI controller having voltage across capacitor ( $v_{dc}$ ) and reference DC voltage ( $v_{dc}^*$ ) as an inputs. The PI controller provides the amplitude  $I_s^*$  of three-phase reference supply current.

In equation (5), the in-phase current unit templates  $u_{ad}$ ,  $u_{bd}$  and  $u_{cd}$  of three-phase currents are derived in-phase with the load voltages.

$$u_{ad} = \frac{V_{La}}{V_{L_{peak}}}; u_{bd} = \frac{V_{Lb}}{V_{L_{peak}}}; u_{cd} = \frac{V_{Lc}}{V_{L_{peak}}} \quad (5)$$

Where  $V_{L_{peak}}$  is the peak value of the supply voltage and it is computed as in equation (6).

$$V_{L_{peak}} = \{2/3(V_{La}^2 + V_{Lb}^2 + V_{Lc}^2)\}^{1/2} \quad (6)$$

In equation (7), in-phase component of reference supply currents  $i_{Sad}^*$ ,  $i_{Sbd}^*$  and  $i_{Scd}^*$  are computed by multiplication of amplitude  $I_{Sd}^*$  with unit current vectors  $u_{ad}$ ,  $u_{bd}$  and  $u_{cd}$ .

$$i_{Sad}^* = I_{Sd}^* u_{ad}; i_{Sbd}^* = I_{Sd}^* u_{bd}; i_{Scd}^* = I_{Sd}^* u_{cd} \quad (7)$$

In equation (8), the quadrature current unit templates  $u_{aq}$ ,  $u_{bq}$  and  $u_{cq}$  of three-phase currents are derived in-phase with the load voltages.

$$u_{aq} = \frac{-u_{bd} + u_{cd}}{\sqrt{3}}; u_{bq} = \frac{u_{ad}\sqrt{3} + u_{bd} - u_{cd}}{2\sqrt{3}}; u_{cq} = \frac{u_{ad}\sqrt{3} + u_{bd} - u_{cd}}{2\sqrt{3}} \quad (8)$$

In equation (9), quadrature component of reference supply currents  $i_{Saq}^*$ ,  $i_{Sbq}^*$  and  $i_{Scq}^*$  are computed by multiplication of amplitude  $I_{Sq}^*$  with unit current vectors  $u_{aq}$ ,  $u_{bq}$  and  $u_{cq}$ .

$$i_{Saq}^* = I_{Sq}^* u_{aq}; i_{Sbq}^* = I_{Sq}^* u_{bq}; i_{Scq}^* = I_{Sq}^* u_{cq} \quad (9)$$

According to the requirement of either power factor improvement, required only in-phase component as a total reference supply current ( $i_s^*$ ) or voltage regulation, required both in-phase component and quadrature component of currents as a total reference supply current given in equation (10),

$$\begin{aligned} i_{Sa}^* &= i_{Sad}^* + i_{Saq}^*; i_{Sb}^* = i_{Sbd}^* + i_{Sbq}^*; \\ i_{Sc}^* &= i_{Scd}^* + i_{Scq}^* \end{aligned} \quad (10)$$

The switching signals are then generated for shunt converter IGBT switches by comparing reference supply currents ( $i_s^*$ ) and the supply currents ( $i_s$ ) and processing the error signal  $i_{error}$  via hysteresis controller, through which the instantaneous three phase source currents track their estimated reference values.

2) **PI Controller:** DC and AC PI controllers are used to find out the amplitude of in-phase  $I_{Sd}^*$  and quadrature  $I_{Sq}^*$  reference supply currents respectively.

The amplitude  $I_{Sd}^*$  of in-phase reference supply currents is computed using PI controller over the average value of DC bus voltage ( $v_{dca}$ ) of the AF and its reference voltage ( $v_{dc}^*$ ). Comparison of average and reference values of dc

bus voltage results in a voltage error, which is expressed as,  $v_{dcError}(n)$ , at  $n^{th}$  sampling instant:

$$v_{dcError}(n) = v_{dc}^*(n) - v_{dca}(n) \quad (11)$$

The perturbed signal  $v_{dcError}(n)$  is fed to PI controller and output  $y_0(n)$  at  $n^{th}$  sampling instant is expressed as:

$$y_0(n) = y_0(n-1) + K_{pd}\{v_{dcError}(n) - v_{dcError}(n-1)\} + K_{id}v_{dcError}(n) = ISd^* \quad (12)$$

Where  $K_{pd}$  and  $K_{id}$  are PI gains. The quantities,  $y_0(n-1)$  and  $v_{dcError}(n-1)$  are the output of the voltage controller and voltage error, respectively, at  $(n-1)th$  sampling instant. The  $I_{Sd}^*$  is amplitude of the reference supply currents considered as output  $y_0(n)$  of PI controller.

Similarly, The amplitude  $I_{Sq}^*$  of quadrature reference supply currents is computed using AC PI controller, comparing the peak value of the supply voltage ( $V_{L_{peak}}$ ) and its reference voltage ( $V_{L_{peak}}^*$ ) results in a voltage error, which is expressed as,  $v_{acError}(n)$ , at  $n^{th}$  sampling instant:

$$v_{acError}(n) = V_{L_{peak}}^*(n) - V_{L_{peak}}(n) \quad (13)$$

The perturbed signal  $v_{acError}(n)$  is fed to PI controller and output  $x_0(n)$  at  $n^{th}$  sampling instant is expressed as:

$$x_0(n) = x_0(n-1) + K_{pq}\{v_{acError}(n) - v_{acError}(n-1)\} + K_{iq}v_{acError}(n) = ISq^* \quad (14)$$

Where  $K_{pq}$  and  $K_{iq}$  are PI gains. The quantities,  $x_0(n-1)$  and  $v_{acError}(n-1)$  are the output of the voltage controller and voltage error, respectively, at  $(n-1)th$  sampling instant.  $I_{Sq}^*$  is the amplitude of the reference supply currents considered as output  $x_0(n)$  of PI controller.

3) **Hysteresis Controller:** The reference supply currents ( $i_s^*$ ) and the actual supply currents ( $i_s$ ) is compared and current error  $i_{error}$  signal is pass through the hysteresis band. According to the error position that is at lower and upper limits the transistors are switched to force the current up and down respectively resulting in the firing pulses at the output.

### III. MATLAB MODEL AND SIMULATION RESULTS

A block diagram of MATLAB model of proposed S-SPQC scheme is shown in Fig. 4 with subsystems, the parameters used in the simulations are shown in the table I.

A diode bridge rectifier R-L load represents the system load. The voltage and current waveforms are shown in fig. 5, the Fast Fourier Transform (FFT) analysis of the responses is done to determine the Total Harmonic Distortion (THD) of the waveforms shown in fig. 6 and fig. 7.

From these results, it can be seen that the source voltage has a distorted waveform (Fig. 5(A)) with a THD value of 12.29% (Fig.6 (A)).It can also be observed that by using SRF technique compensating voltage (Fig. 5(B)) was extracted properly and provides the clean load voltage (Fig. 5(C)) at the point of common coupling with a THD value of 0.57% (Fig. 6 (B)) i.e. 95.36 % voltage harmonics was compensated.

It can be seen that the load current has a distorted waveform (Fig. 5(D)) with a THD value of 25.77% (Fig. 7(A)).It can also be observed that by using ICC technique compensating current (Fig. 5(E)) was extracted properly and supplies the pure source current (Fig. 5(F)) with a THD value of 0.27% (Fig.7 (B)) i.e. 98.95% current harmonics was compensated. It can also be seen that the source current settles to its steady state value within five cycles Furthermore, it can be seen that, for sudden load change (rise) the dc link voltage dips to 695V and settles at its reference value within three cycles (Fig. 5(G))

TABLE I. S-SPQC SYSTEM SIMULATION PARAMETERS

Simulation Blocks	Parameters	Values
Source	Voltage	$V_s$ 400 V
	Frequency	$f$ 50 Hz
	Source Resistance	$R_s$ 0.03 $\Omega$
	Source Inductance	$L_s$ 0.20 mH
	Total Harmonic Distortion	THD $_{V_s}$ 12.29 %
Non-Linear Load	Line Inductance	$L_{chock}$ 2 mH
	dc Inductance	$L_L$ 10 mH
	dc Resistance	$R_L$ 30 $\Omega$
	Total Harmonic Distortion	THD $_{I_L}$ 25.77 %
DC Link	Voltage	$V_{DC}$ 700 V
	Capacitor	$C_{DC}$ 2200 $\mu$ F
Shunt APF	Line Inductance	$L_p$ 3.5 mH
	Ripple Filter Resistor	$R_p$ 5 $\Omega$
	Ripple Filter Capacitor	$C_p$ 10 $\mu$ F
Series APF	Line Inductance	$L_s$ 3.5 mH
	Ripple Filter Resistor	$R_s$ 5 $\Omega$
	Ripple Filter Capacitor	$C_s$ 20 $\mu$ F
ICC block	Proportional Gain	$K_{pd}$ 0.2 --
	Integral gain	$K_{id}$ 3.2 --
	Proportional Gain	$K_{pq}$ 0.32 --
	Integral gain	$K_{iq}$ 3.4 --
SPWM block	Proportional Gain	$K_p$ 1.2 --
	Integral gain	$K_i$ 4.7 --

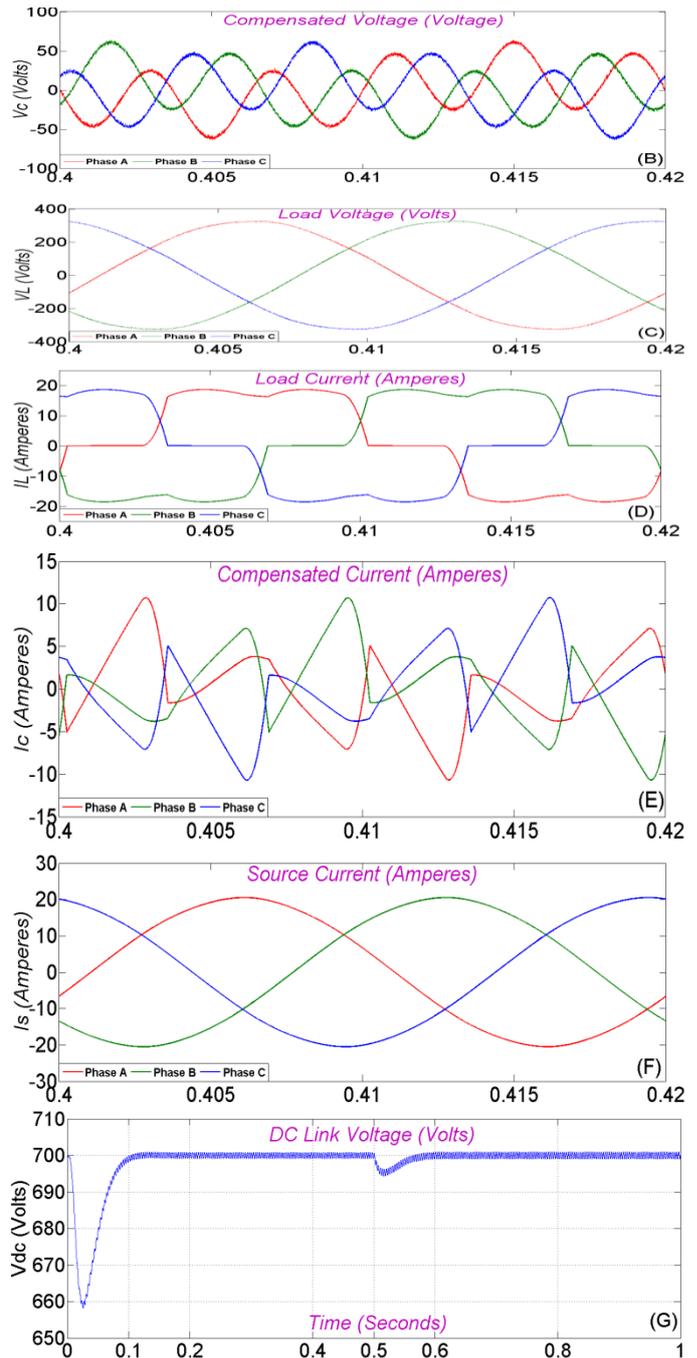


Figure 5. Voltage and current waveforms for distorted mains voltage and harmonically polluted currents

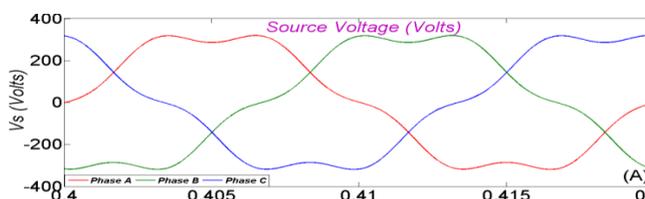


TABLE II. S-SPQC SIMULATION RESULTS OF VOLTAGE REGULATION FOR VARIOUS CONDITIONS

	Phase s	Without Quadrature component of reference current						With Quadrature component of reference current					
		Normal Load		Load Variation (Rise)		One Line open Fault		Normal Load		Load Variation (Rise)		One Line Open Fault	
		RMS Value	% THD	RMS Value	% THD	RMS Value	% THD	RMS Value	% THD	RMS Value	% THD	RMS Value	% THD
Source Voltage (Vs)	A	224	12.64	220.7	12.83	227.9	12.43	223.8	12.65	220.8	12.82	227.3	12.46
	B	224	12.64	220.7	12.83	227.9	12.43	223.9	12.65	220.8	12.82	227.5	12.46
	C	224	12.64	220.7	12.83	227.7	12.43	223.8	12.65	220.8	12.81	227.4	12.45
Voltage At PCC (VL)	A	231.9	0.34	228.5	0.35	233.8	0.50	<b>230.6</b>	0.53	<b>230.2</b>	0.43	<b>230.8</b>	0.77
	B	231.8	0.36	228.5	0.35	233.4	0.51	<b>230.7</b>	0.45	<b>229.9</b>	0.39	<b>230.9</b>	0.69
	C	231.9	0.34	228.5	0.33	233.5	0.49	<b>230.5</b>	0.43	<b>230.1</b>	0.40	<b>231.2</b>	0.66

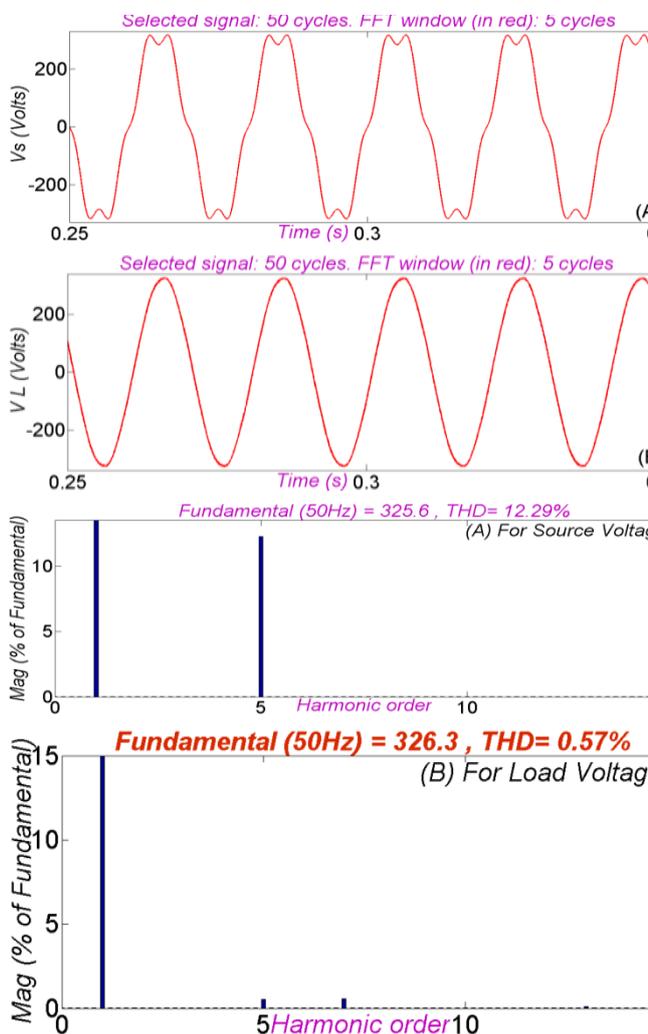


Figure 6. FFT analysis: (A) source voltage (B) load voltage

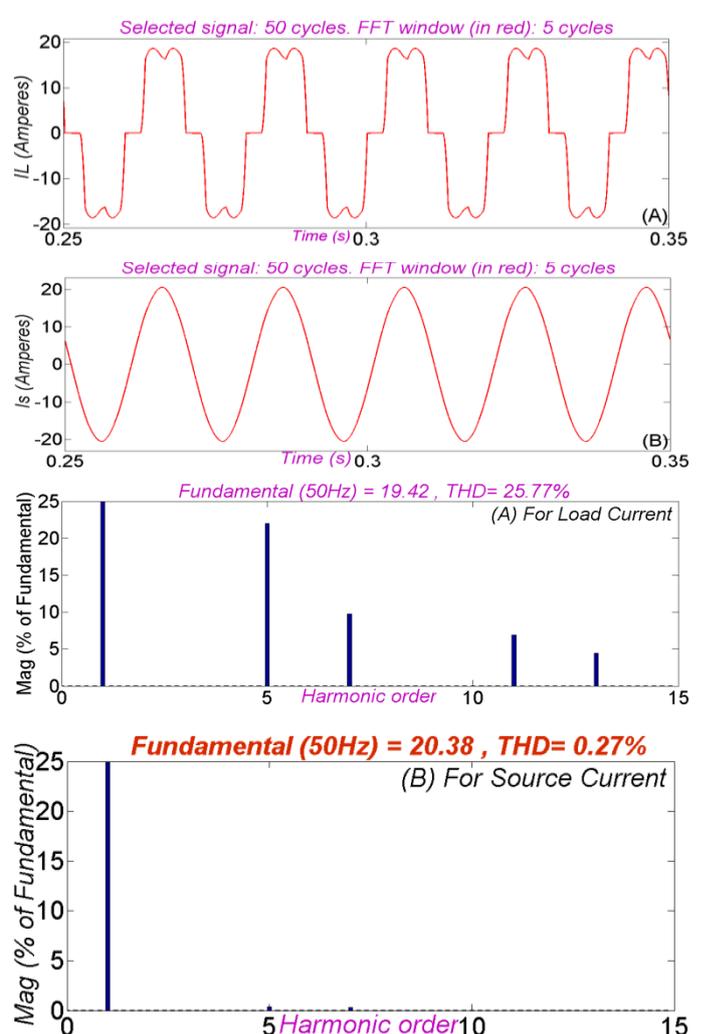


Figure 7. FFT analysis: (A) source current (B) load current

#### IV. CONCLUSION

This paper has presented a new control strategy for the S-SPQC system, which mainly compensate reactive power and voltage and current harmonics in the load under distorted mains voltage and load current conditions. The proposed control strategy requires only source current and load voltage measurement for shunt APF based on the indirect current control technique. The synchronous reference frame technique was used by measuring mains voltage and filter voltage for series APF so it reduces the number of measurement sensors. The simulation results highlighted that, the above control algorithms eliminate the impact of distortion of load current on the power line and isolate the loads voltages and source voltage.

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#### BIOGRAPHIES



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**U. Gudar**, aged 73 years has obtained his B.E. in 1962, M.E. in 1966 and Ph.D in 1983. He published three papers at International level, and presented / published 32 other papers at National seminars / Journals. After superannuation in 1999, the All India Council for Technical Education (AICTE) has awarded Emeritus Fellowship for carrying out research work on the topic, "Measures for Power Quality Improvement". The author is a Fellow of Institution of Engineers (India) in their Computer Engineering Division. He is a Senior member of IEEE in their power engineering society. Currently he is working as a Professor in Annasaheb Dange College of Engineering and Technology, Ashta (MS).