Design and Simulation of 8255 Programmable Peripheral Interface Using VHDL

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Abstract: The 8255A programmable peripheral interface PPI) implements a general-purpose I/O interface to connect peripheral equipment to a microcomputer system bus. The core's functional configuration is designed by VHDL code and designed input signal (Test bench) for PPI 8255, which is generated by VHDL code. Simulated result is verified for one 8-bit Peripheral Ports - Ports A, three programming modes for Peripheral Ports: Mode 0 (Basic Input/output programmable I/O lines .Also verified simulated and synthesized result for PPI 8255. All designed is done by using Xilinx ISE10.1i.

Keywords: VHDL Code, MOS, MCS85, PPII.

I. INTRODUCTION

The 8255 PPI The 8255 Programmable Peripheral Interface chip is a peripheral chip originally developed for the Intel 8085 microprocessor, and as such is a member of a large array of such chips, known as the MCS-85 Family. This chip was later also used with the Intel 8086 and its descendants. It was later made (cloned) by many other manufacturers. It is made in DIP 40 and PLCC 44 pins encapsulated versions. This chip is used to give the CPU access to programmable parallel I/O, and is similar to other such chips like the Motorola 6520 PIA (Peripheral Interface Adapter) the MOS Technology 6522 (Versatile Interface Adapter) and the MOS Technology CIA (Complex Interface Adapter) all developed for the 6502 family. Other such chips are the 2655 Programmable Peripheral Interface from the Signe tics 2650 family of microprocessors, the 6820 PIO (Periphera PIO (Peripheral Input/output) from the Motorola 6800 family, the Western Design Center WDC 65C21, an enhanced 6520, and many others. The 8255 is widely used not only in many microcomputer/ microcontroller systems especially Z-80 based, home computers such as SV-328 and all MSX, but also in the system board of the best known original IBM-PC, PC/XT, PC/jr, etc. and clones. However, most often the functionality the 8255 offered is now not implemented with the 8255 chip itself anymore, but is embedded in a larger VLSI chip as a sub function. The 8255 chip itself is still made, and is sometimes used together with a micro controller to expand its I/O capabilities.

ABOUT VHDL

In this project we have implemented 8255 PPI using Xilinx ISE 10.1i Software. The coding is done in VHDL language. VHDL (VHSIC hardware description language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field programmable gate arrays and integrated circuits. VHDL was originally developed at the behest of the U.S Department of Defense in order to develop an alternative to huge, complex manuals which were subject to implementation specific details. VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design.

II. OVERALL ARCHITECTURE AND DESCRIPTION:

A. PPI - Programmable Peripheral Interface

The 8255A programmable peripheral interface (PPI) implements a general-purpose I/O interface to connect peripheral equipment to a microcomputer system bus. The core's functional configuration is programmed by the system software so that external logic is not required to interface peripheral devices.

Features:

➢ 3 8-bit IO ports PA, PB, PC

➢ PA can be set for Modes 0, 1, 2. PB for 0, 1 and PC for modev0 and for BSR. Modes 1 and 2 are interrupting driven.

➢ PC has 2 4-bit parts: PC upper (PCU) and PC lower (PCL),each can be set. Independently for I or O. Each PC bit can be set/reset individually in BSR mode.
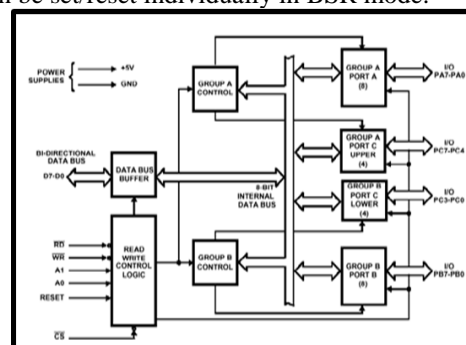

Fig. 1: Architecture of 8255 PPI

➢   Address/data bus must be externally demultiplexed.
➢   TTL compatible.
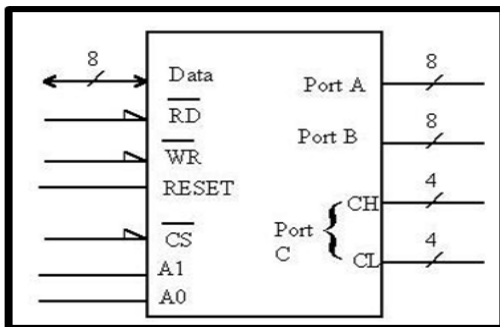➢   Improved dc driving capability.

Fig. 2: Pin diagram of 8255 PPI

The IC used for interfacing is the 8255 PPI. This chip is designed and manufactured by Intel. The 8255 Interface Adapter is a programmable peripheral interface device designed for use in microcomputer interfacing systems. It is a general purpose I/O device that can interface any TTL compatible peripheral device to a microcomputer system. The 8255 has 24 pins of I/O, programmable and configurable by software, in two groups of 12 pins that are used in three separate modes of operation (Brey, 1995). The Interface Adapter is selected by its CS line for programming and for reading and writing to a port. Port assignment and register selection is accomplished through the A1 and A0 pins. Table 2 shows the I/O port assignments used programming and access the I/O ports.

Table 1: Function of Port A, B, C and CWR

A1	A2	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

B. Programming with 8255 PPI
The 8255 has 3 8-bit ports (A, B and C), each of which can have a different I/O Status (i.e. input or output). Port C can also be programmed to operate in two halves. (As two separate 4-bit ports). The functional configuration of each port is programmed but the system software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset", etc, that initializes the functional configuration of the 8255. There are 3 basic modes of operation under which the ports can function. Mode 0 - Basic Input/ output Mode 1 - Strobed input/output (Not used by SVI) Mode 2 - Bi-Directional Bus (Not used by SVI) in some of these modes port C is used as a control/status port for port A or B. It can be used to confirm when data transfer may take place, and reflect any other flags. The 8255 PPI is therefore supplied with the added option for the user to set or reset any individual bits in port C. The I/O status, mode of operation and bit setting is defined by the 8255 PPI control byte. (The control byte is accessed using port 97H, 8255 Control port) The ports may be accessed separately by the CPU. Port A is accessed using port 98H, Port B is accessed using port 99H, Port C is accessed using port 96H.

C. Use 8255 PPI in VHDL programming
8255 PPI is used in VHDL; we use VHDL code as in input and to give the output in simulated test bench waveform. As we know that, this is also perform in the matlab and P-spice technology and in this project we are using new advance technology called VHDL to give simulated test bench waveform of 8255 PPI. The codes for the different modules are written in VHDL and are simulated using Xilinx ISE 10.1.
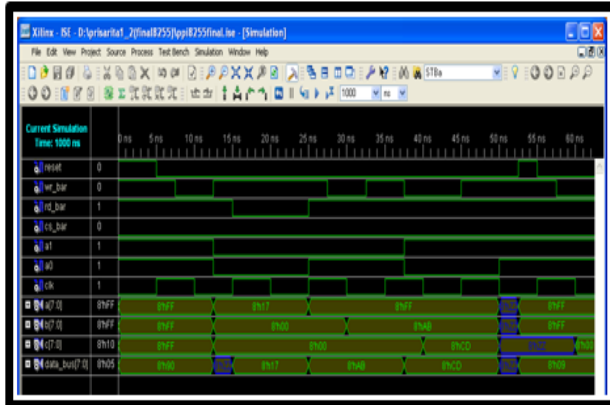
Results obtained:
1.   RTL View of 8255 PPI Architecture
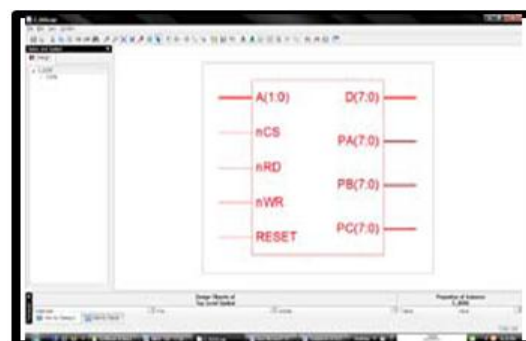
2.   RTL View of 8255 PPI Core Internal
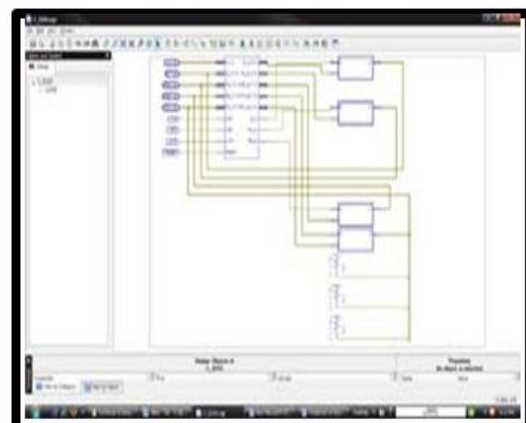
3.   Simulated Test bench Waveform 8255 PPI Architecture Mode 0

REFERENCES

[1] Harris Semiconductor, "CMOS programmable Peripheral Interface", Product Specification, June 1998.

[2]. Paul, "8255 PPI IBM PC Interface Card", Tutorial, Nov 2000.

[3] Intel, "Programmable Peripheral Interface", Data Sheet, 1999.

[4] T.C. Manjunath, S. Janardhanan, N.S. Kubal, "Simulation, Design, Implementation and Control of a Welding Process Using Micro – controller", Paper presentation at Institute of Technology Bombay, Powai, Mumbai.

[5] Pradeep Kumar Jaisal, Anant G. Kulkarni, "Design of Time Triggered Shared Bus Architecture Using Very High Speed Integrated Circuit Hardware Description Language (VHDL)",Paper Published at International Journal of Electronics and Computers, Vol. 2, No. 2, pp. 353-364.

[6] . Pradeep Kumar Jaisal, Anant G. Kulkarni, **"**Design and Simulation of 8255 Programmable Peripheral Interface Adapter Using VHDL" paper published in IJCST Vol. 2, Issue 1, March 2011.

[7] Ramesh S. Gaonkar,"Microprocessor   Architecture,Programming and Application with 8085 ,"Wiley Eastern Ltd.,5ᵗʰ Edition.

[8] D. E. Thomas and P. Moorby. *The Verilog Hardware Description Language*. Kluwer Academic, 1991.

[9] IEEE. *IEEE Standard VHDL Language Reference Manual*. IEEE, 1988.

[10] Aldec active-hdl tools. www.aldec.com.