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Design Approach for Simulation of Complex Mathematical Models

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Abstract: Many applications that are DSP based or certain communication application require mathematical modelling for their easy understanding and analysis. Due to its complexity Pure HDL is unable to simulate. Also it terms to be costly and time consuming process.

We propose an alternative approach based on mixed HDL-Simulink platform. Basic properties of the simulation process in Simulink are addressed. The problems of data and signal transfers, driving samples, synchronization and entire communication between HDL and Simulink are described in details. A methodology for implementing DSP based or communication applications on a field programmable gate arrays (FPGA) using Xilinx System Generator (XSG) for Matlab. Implementation of examples related to DSP and Communication based designs are presented.

Keywords: FPGA(Field Programmable Gate Arrays),XSG(Xilinx System Generator),VHDL.

I. INTRODUCTION

Today the main challenge that is faced by the electronic equipment designers is to deliver quality products to the market as quickly as possible. The next requirement concerns the devices reliability and flexibility i.e. modifications and changes have to be possible without significant difficulties. Moreover the complexity of such systems makes impossible to manually control the entire design - main operations like high level synthesis and technology mapping are executed automatically – only some slightly changes are possible. Because of these facts the problem of a proper formulation and implementation of the design task on the high level of abstraction is very crucial.

The Hardware Description Languages (HDLs) have been developed for several years in this field. The HDLs and automated tools based on them have given new abilities to designers, however now they seen to be not sufficient. Now we are looking for tools that deal with models and descriptions on higher levels of abstraction and we would like to describe the entire system as a one piece i.e. without its initial, manual decomposition into the hardware and software. The terms of system level design, co-design and co-simulation have been well known for several years. The complexity of the systems has a strong impact on the models that are expected to reflect the functionality and timings of the real devices.

We propose an approach based on mixed HDL-Simulink platform. Basic properties of the simulation process in Simulink are addressed. Many applications that are DSP based or certain communication application require mathematical modelling for their easy understanding and analysis. In consequence, the abstract models are very complicated and a designer has to implement very sophisticated algorithms requiring many computational tasks. HDL languages like VHDL or Verilog are designed for different purposes. Although, it is possible to describe every algorithm in these tools, sometimes it is very difficult, needs lot skills and is not effective and very time consuming. That is why EDA vendors are working on tools which can combine different abilities in one environment. Our work concerns the approach that proposes a tool enabling effective simulation of complex abstract mathematical models.

Matlab-Simulink is an environment for multidomain simulation and Model-Based Design for dynamic and embedded systems. Matlab-Simulink is used in this application as the high level development tool in the design process. Xilinx System Generator, is a system-level modelling tool from Xilinx that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modelling environment well suited for hardware design. The software automatically converts the high level system DSP block diagram to RTL. The result can be synthesized to Xilinx FPGA technology using ISE tools. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. It also provides a system integration platform for the design of DSP FPGAs that allows the RTL, Simulink, MATLAB and C/C++ components of a DSP system to come together in a single simulation and implementation environment. System Generator supports a box block that allows RTL to be imported into Simulink and cosimulated with either ModelSim or Xilinx ISE Simulator.

II. BACKGROUND

After a thorough literature review, some of the most valuable recent documents and papers are,

As Author Adam Milik and Andrzej Pulka papers presented [1] methodology has been implemented and tested in mixed Active-HDL 7.2 and MATLAB 7.01 environments, and the experiments has been done on

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WINDOWS XP platform working on Pentium 4 Core Duo (2GHZ/1GB). The designed and implemented cosimulation environment is dedicated to testing of models hardware in mathematical modeling system developed with MATLAB and Simulink. Time taken it will be more, to improve upon this major factor, they propose to use the ALDEC Active- HDL simulator together with the Mathworks Simulink [5]. The construction of accurate and appropriate model of the object in HDL is very difficult, and the object model translation from the mathematical representation into HDL is challenging, time-consuming and error prone task.

The paper presented [2] a theoretical background overview of the digital communication systems and the BPSK modulation and demodulation. The purposed design is the BPSK system. The BPSK modulation and demodulation represents an important modulation technique in terms of signal power. The BPSK system is simulated using Matlab/ Simulink environment and System Generator, a tool from Xilinx used for FPGA design as well as implemented on two Spartan 3E Starter Kit boards. The first board behaves as a modulator and the second as a demodulator. The modulator and demodulator algorithms have been implemented on FPGA using the VHDL language on Xilinx ISE 12.3. The local clock oscillator of the board is 50MHZ which corresponds with a period of 20ns. The frequency of the BPSK carrier is 31,250 kHz. Both, the modulator and demodulator, have been designed and simulated.

The paper presented [3] the simulation of a BPSK Modulator using Matlab/ Simulink environment an system Generator, a tool from Xilinx used for FPGA design as well as the implementation of the modulator on a Spartan 3E Starter Kit board. The modulator algorithm has been implemented on FPGA using the VHDL language on Xilinx ISE 12.3. The modulated signal obtained from simulations was compared with the signal obtained after implementation.

In this paper a methodology for implementing DSP based or communication applications on a field programmable gate arrays (FPGA) using Xilinx System Generator (XSG) for Matlab. For that purpose we are used mixed HDL simulink platform. This project shows the ability of to be used for the approximation of Simulation of Complex Mathematical Models Using Mixed HDL Platform .

III. PROPOSED WORK

A. MATLAB:

Matlab is a high-level technical computing language and interactive environment for algorithm development, data visualization, data analysis, and numeric computation. In addition to the intellectual property functions provided in Matlab, the software packet is uniquely adept with vector and array based waveform data at the core of algorithms, which is suitable for applications such as image and video processing. Matlab-Simulink is an environment for multi-domain simulation and Model-Based Design for dynamic and embedded systems. It provides an interactive graphical environment, event-driven simulator, and extensive library of parameterizable functions that allow design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing, image and video processing. Matlab-Simulink is used in this application as the high level development tool in the design process.

B. MATLAB Simulink:

MATLAB software tool is used for developing program for different equations and algorithms. With the help of MATLAB tool it is more convenient to use simulink library where in various readily available block sets are available by which any system can be easily designed. The main advantage of MATLAB is that it can be easily interfaced with Code Composer Studio (CCS 3.1). MATLAB, developed by MathWorks Inc., is a software package for high performance numerical computation and visualization. The combination of analysis capabilities, flexibility, reliability, and powerful graphics makes MATLAB the premier software package for electronics engineers. It is an interactive tool for modelling, simulating, and analyzing dynamic systems. It enables you to build graphical block diagrams, simulate dynamic systems, evaluate system performance, and refine your designs. Simulink integrates seamlessly with MATLAB, providing you with immediate access to an extensive range of analysis and design tools. These benefits make Simulink the tool of choice for control system design, DSP design, communications system design, and other simulation applications. Simulink systems are often referred to as dynamic systems. Simulink can be used to explore the behavior of a wide range of real-world dynamic systems, including electrical circuits, shock absorbers, braking systems, and many other electrical, mechanical, and thermodynamic systems.

C. System Generator:

Matlab-Simulink is an environment for multidomain simulation and Model-Based Design for dynamic and embedded systems. Matlab-Simulink is used in this application as the high level development tool in the design process. Xilinx System Generator, is a system-level modeling tool from Xilinx that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modelling environment well suited for hardware design. The software automatically converts the high level system DSP block diagram to RTL. The result can be synthesized to Xilinx FPGA technology using ISE tools. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. It also provides a system integration platform for the design of DSP FPGAs that allows the RTL, Simulink, MATLAB and C/C++ components of a DSP system to come together in a single simulation and implementation environment. System Generator supports a box block that allows RTL to be imported into Simulink and cosimulated with either ModelSim or Xilinx ISE Simulator.

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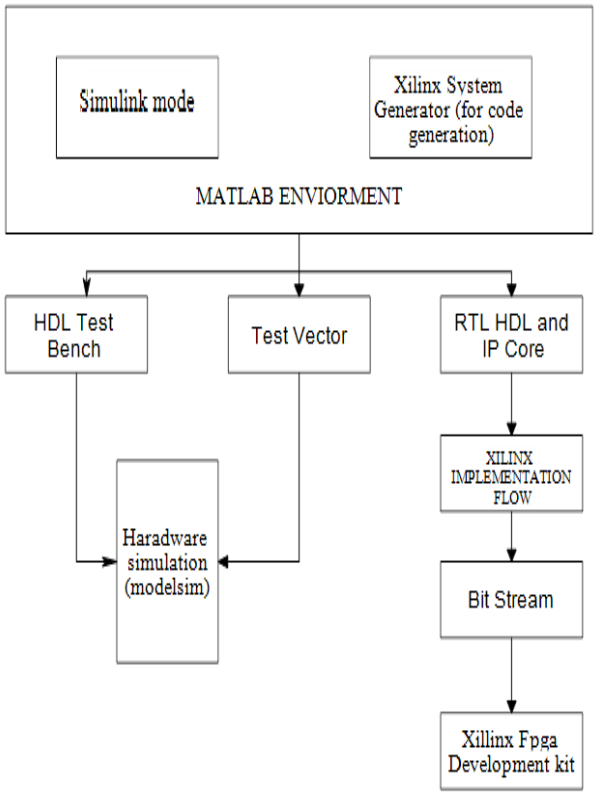

Figure: Block Diagram of System Generator

D. Hardware-Software Cosimulation:

System Generator the use of simulates automatically launching an HDL simulator, generating additional HDL as needed (analogous to an HDL testbench), compiling HDL, scheduling simulation events, and handling the exchange of data between the Simulink and the HDL simulator. This is called HDL co-simulation. System Generator provides hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a Simulink simulation. "Hardware Co-Simulation" compilation targets automatically create a bit-stream. When the system design is simulated in Simulink, results for the compiled portion are calculated in actual FPGA hardware, often resulting in significantly faster simulation times while verifying the functional correctness of the hardware. System Generator for DSP supports Ethernet as well as JTAG communication between a hardware platform and Simulink.

System Generator provides a generic interface that uses JTAG and a Xilinx programming cable (e.g., Parallel Cable IV or Platform Cable USB) to communicate with FPGA hardware. The model with the JTAG-based hardware co-simulation block implemented on Virtex 5 platform. Point-to-point Ethernet co-simulation provides a straightforward high-performance co-simulation environment using a direct, point-to-point Ethernet connection between a PC and FPGA platform. The target FPGA chip is Xilinx Spartan 3A DSP 3400XC3SD3400A-4FGG676C and Virtex 5 xc5vlx50-1ff676. The optimization setting is for maximum clock speed. Xilinx system generator has a unique hardware in the loop co-simulation feature that allows designers to greatly accelerate simulation while simultaneously verifying the design in hardware.

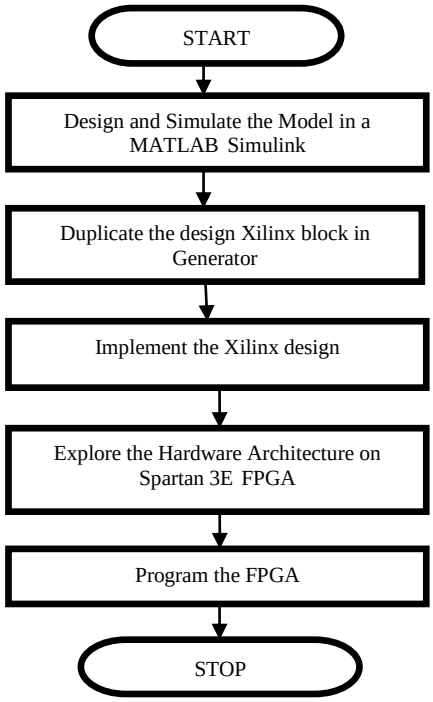

FIG: DESIGN FLOW CHART

Sometimes it is important to add one or more existing HDL modules to a System Generator design. The System Generator allows VHDL, Verilog, to be brought into a design. When System Generator compiles, it automatically wires the imported module and associated files into the surrounding netlist. Xilinx system generator is a very useful tool for developing computer vision algorithms. It could be described as a timely, advantageous option for developing in a much more comfortable way than that permitted by VHDL or Verilog hardware description languages (HDLs).

IV. CONCLUSION

In this paper we present the system to simulate complex mathematical models. The proposed methodology has been tested with Xilinx System Generator (XSG) and MATLAB environments. The basic concepts of creating a design using System Generator within the model-based design flow provided through Simulink. First to design and simulate the model in a MATLAB Simulink. Then the design Xilinx block in system generator and we take the Xilinx executable specification through the full implementation flow. And Explore the Hardware Architectures on Spartan 3E FPGA to achieve the best performance. Finally in the program run FPGA.

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