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Review Paper on Memristor MOS Content Addressable Memory

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Abstract: The ongoing development of networks such as internet also takes about the need for being able to design new component or circuits that are able to exist together with CMOS process technology as CMOS scaling begins to slow down. This paper provides a review on the various memory devices and basic introduction of the proposed Memristor based content addressable memory (CAM) for future high performance search engine using VLSI technology. Memristor is nonlinear resistor which acts as memory. Therefore designing MCAM based on VLSI improves the speed, low power consumption, and reduces size. Further designing CAM based on memristor increases the packing density, provides for the new approaches towards power management through disabling CAM blocks without loss of stored data, reduces power dissipation, and has scope for speed improvement as the technology matures

Keywords: Content addressable memory (CAM), memory; memory-resistor based CAM (MCAM), MICROWIND3.1 software, modeling.

I. INTRODUCTION

Internet is the most popular medium to communicate with the visitors, customers and other businessmen for branding and promoting a business. Now everyone is depending on the internet to seek anything they need. In such a world it becomes necessary for every business to market itself in the online world, as it is a popular medium that is used by almost everyone in the world. All businesses are making efforts to build a large customer base by means of internet. For getting large customer base it is necessary to be indexed in the search engines like Google, Yahoo, Bing and MSN etc. as internet users search any information they need through search engines. The primary requirement of this search engines is memory require storing data and also high operating speed. Concerning this there is large development has done in memory devices. Power, area and time are the major milestones for VLSI circuits. This paper provides new approach for non-volatile Memristor-based Content Addressable Memory MCAM cell using memristor with CMOS processing technology in order to get high speed read/write operations within high packing density and low power dissipation. A typical content addressable memory cell forms a SRAM cell that has two p-type MOS transistors. Construction of a SRAM cell that use memristor technology, which has a non volatile memory behaviour and can be fabricated as an extension to a CMOS process technology with nanoscale geometry, addresses the main thread of current CAM research towards reduction of power consumption. The design of a CAM cell is based on fourth passive circuit element, the memristor predicted by Chua in 1971 and generated by kang. Chua postulated that a new circuit element defined by the single valued relationship "dϕ=Mdq" must exist; where by current moving through memristor is proportional to the flux of magnetic field that flows through the material.

II. RELATED WORK

From the rigorous review of related work and published literature, it is observed that many researchers have designed MOS content addressable memory by applying different techniques. Researchers have undertaken different systems, processes or phenomena with regard to design and analyse MOS content addressable memory and attempted to find the unknown parameters. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing MOS content addressable memory with CMOS/VLSI technology. Data processing/storing that involves many search operations performed by software consumes enormous time. This is a hindrance to high-speed data processing. A fully parallel content addressable memory (CAM) compares search data with storage data in a parallel fashion, and is extremely suitable for high-speed data searching. A search operation carried out by a fully parallel CAM is several hundred times faster than that performed by software. Therefore, there have been many studies that have addressed the applicability of CAM's to artificial intelligence (AI) machines, data-base systems, and so on in which search operations are conducted frequently. Conventional CAM's use a static CAM cell, which keeps storage data in a latch, to accomplish a stable operation it was discussed by T. Nikaido, T. Ogura, S. Hamagrrchi, and S. Muramoto, in their publish paper in 1983 Static CAM cells, However, the speed of a CAM comes at the cost of increased silicon area and power consumption, two design parameters that designers strive to reduce. As CAM applications grow,

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demanding larger CAM sizes, the power problem is further exacerbated. Reducing power consumption, without sacrificing Speed or area, is the main thread of recent research in large-capacity CAM. Several techniques have been proposed to reduce the power consumption in CAMs. In Jun. 1997 C. Zukowski and S. Wang, published a paper in which they used a selective precharge CAM which reduces the power by precharging the match lines only if there is match in the selected bits of the words. The number of selected bits is optimized for minimum average energy the power consumption is reduced by shutting down the power for redundant comparisons but there was problem of voltage swing of match line occurred. Later on H. Miyatake, M. Tanaka and Y. Mori published a paper in which voltage swing of ML is reduced by charging it through an NMOS transistor and discharging it by PMOS comparison logic. A precomputation-based CAM was recently proposed by C. S. Lin, J.C. Chang and B. D. Liu which reduces the power by extracting a smaller size parameter from each word. Hence, the power reduction is achieved at the expense of slower search speed. Moreover, increased complexity due to the additional logic makes it difficult to cascade multiple CAMs. Recently, a current-race sensing scheme is proposed that reduces the power. Latter on Nitin Mohan and Manoj Sachdev published a paper in which they presented a dual ML TCAM scheme they showed that by theoretical analysis and simulation results that the dual ML TCAM results in significant power reduction (up to 43%) at the expense of small trade-off in speed (4%). Verma and chandrakasan demonstrate that at very low supply voltages the static noise margin for SRAM will disappear due to process variation to address the low SNM for subthreshold supply voltage. This means, there is a need for significant increase in silicon area to have reduced failure when the supply voltage has been scaled down.

Memory processing has been considered as the pace-setter for scaling a technology. A number of performance parameters including capacity (that relate to area utilization), cost, speed (both access time and bandwidth), retention time, and persistence, read/write endurance, active power dissipation, standby power, robustness such as reliability and temperature related issues. Memristor was originally envisioned in 1971 by circuit theorist Leon Chua, Memristor - the missing circuit element. IEEE Trans. Circuit Theory 18, 507–519 (1971). He describe memristor as a missing non-linear passive two terminal electric component relating electric charge and magnetic flux linkage Leon Chua more recently argued that the definition should be generalized to cover all forms of 2-terminal non-volatile memory devices based resistance switching effects although some experimental evidence contradicts this claim. In 2008 team at HP labs announced the development of switching memristor based on a film of titanium dioxide these devices are intended in nanoelectric memory, and computer logic. Chua postulated that a new circuit element defined by the single-valued relationship must exist, whereby current moving through the memristor is proportional to the flux of the magnetic field that flows through the material. This paper explore the design of CAM based on memristor using VLSI technology. The memristor behaves as a switch, much like a transistor. However, unlike the transistor, it is a two-terminal rather than a three-terminal device and does not require power to retain either of its two states so due to this property of memristor there is further reduction in power consumption than that of conventional CAM. Memristor changes its resistance between two values and this is achieved via the movement of mobile ionic charge within an oxide layer, furthermore, these resistive states are non-volatile. This behavior is an important property that influences the architecture of CAM systems, where the power supply of CAM blocks can be disabled without loss of stored data. Therefore, memristor-based CAM cells have the potential for significant saving in power dissipation.

In our paper we are designing model operating at 32 nm, this further improves the speed of search engine. On January 2009 Di ventra, Pershin, Chua extended the notion of memory system to capacitive and inductive element namely capacitors and inductors whose properties depend on the state and history of system. On April 20 Memristor-based content addressable memory (MCAM) was introduced. In October 2011 Tse demonstrated printed memristive counters based on solution processing, with potential applications as low-cost packaging components (no battery needed; powered by energy scavenging mechanism). On April 23, 2013 Valov, et al., argued that the current memristive theory must be extended to a whole new theory to properly describe redox-based resistively switching elements (ReRAM)**.** IEEE transactions on very large scale integration (VLSI) systems, by Kamran Eshraghian, Kyoung-Rok Cho, Omid Kavehei, Soon-Ku Kang, Derek Abbott and Sung-Mo Steve Kang, explore conceptualization, design, and modeling of the memory/compare cell as part of a memristor-based content addressable memory (MCAM) architecture using a combination of memristor and n-type MOS devices. It is seen that by designing CAM based on memristor using VLSI technology improves low power dissipation the non-volatile characteristics of the memristor provides storage of data during power supply cut-off. Further use of VLSI technology provides reduction in silicon area and improved speed of the searching engine.

III. PUBLISHED MCAM STRUCTURE

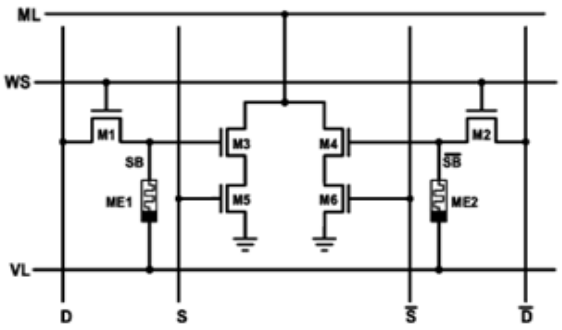

Fig.3.1 published 6TSRAM using memristor

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A CAM cell serves two basic functions: "bit storage" and "bit comparison "there are variety of approaches in design of basic cell such as NOR based match line, NAND based match line, etc. This paper reviews the properties of conventional SRAM based CAM and provides a possible approach for the design of content addressable memory based on memoristor as shown in fig 3.1. Unfortunately, CAM is a type of volatile memory. So that including memristors, a passive element "memory resistor", in CAM cells for bit storing provides nonvolatility property which ensures that data can be retained after the power supply is removed enabling new possibilities in system design including the all important issue of power management.

IV. PROPOSED WORK

Memristor is a new- found fundamental circuit element whose behavior is predicted using either the charge dependant function called memristance or flux dependant function called memductance. Therefore, it is important to find the memristance or memductance function of memristor. The methodology suggest first doing several experiment with a memristor using a square-wave signal to acquire data and then using algorithm inspired by the experiment on ionic memristor. The keywords use for this design is content addressable memory (CAM), memory; memory-resistor based CAM (MCAM), MICROWIND3.1 software. Every step of design follows the design flow of software as mentioned in fig 4.1

The design methodology will be according to VLSI backend design flow. To achieve the proposed target following steps are included in the design and analysis of proposed MCAM.

1. Schematic design of proposed MCAM using CMOS transistors.
2. Performance verification of the above for different parameters.
3. CMOS layout for the proposed MCAM using VLSI backend.
4. Verification of CMOS layout and parameter testing.

If the goal is achieved for all proposed parameter including detail verification, sing off for the design analysis and design will be ready for IC making. If detail verification of parameters would not completed then again fallow the first step with different methodology. To achieve the proposed MCAM, different methodology and techniques can be used for research. The MICROWIND3.1 program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module.

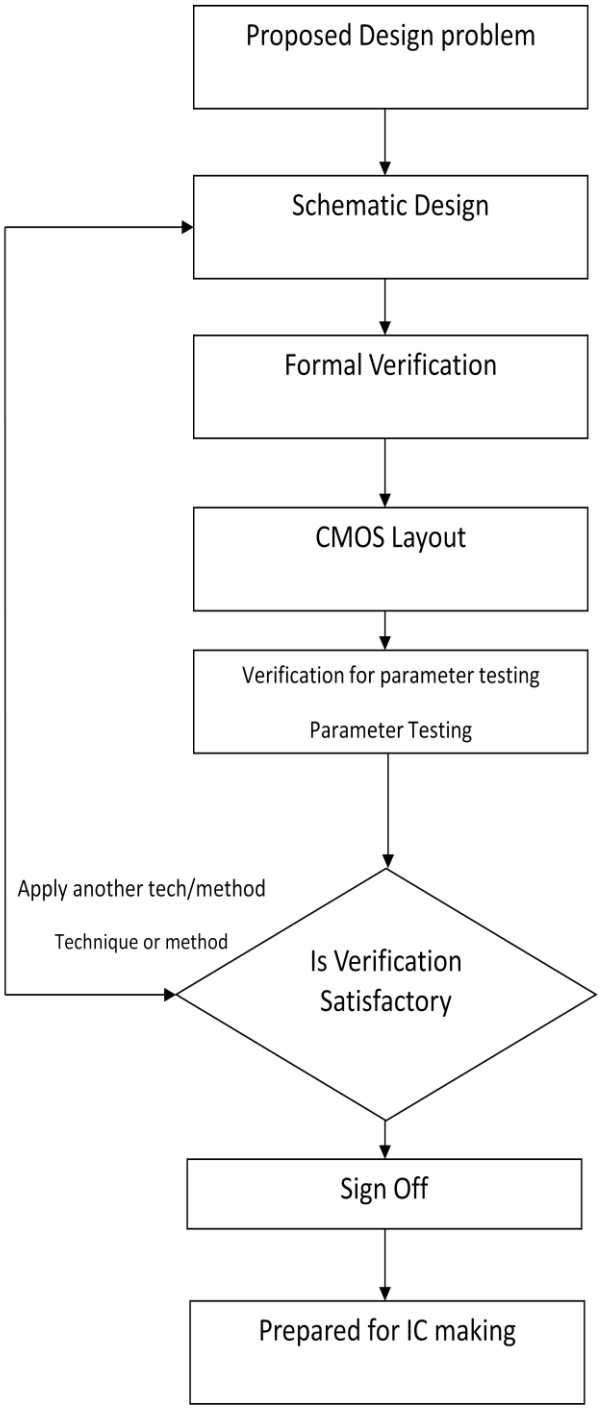

Fig 4.1 design flow chart.

We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and simulation by pressing one single key and the analog simulator produces voltage and current curve immediately.

The fig 4.2 shows the 6T-SRAM cell design using MICROWIND3.1software In our work we design a 6TSRAM on MICROWIND3.1 window as we are using VLSI technology. Here we are replacing MOS circuitry by CMOS. The fig c. shows the 6TSRAM cell which consists of 6 transistor. They are connected by metal 1 shown in

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blue color and contact is made by using different contact such as metal-gate contact, metal1-metal2 contact.

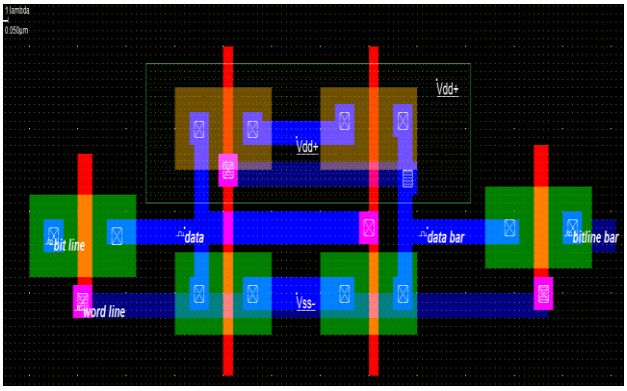

Fig 4.2. layout of 6TSRAM on MICROWIND3.1 software

V. CONCLUSION

The non-volatile characteristic and nanoscale geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data. Our simulation results will show MCAM approach provides a 45% reduction in silicon area when compared with the SRAM equivalent cell .As we are designing our project at 32nm technology so there is further improvement in speed.

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