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Neuro-Fuzzy Buck Boost Converter Implement on FPGA

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Abstract: The DC-DC power converters are widely used. However, the controller design for DC-DC power converters cannot easily design if load is dynamics vary widely. Therefore a Field Programmable Gate Array (FPGA) is proposed to build a neuro fuzzy system for controlling a nonlinear buck boost converter. A Very High speed integrated circuit Hardware Description Language (VHDL) has been used to implement the proposed controller. The main purpose behind implementation of the NF controller in VHDL is to minimize the hardware implementation cost of the generic NF controller for use in industrial applications. Xilinx ISE 13.1 program has been used as programming environment to type and synthesis the VHDL codes that described the neuro-fuzzy controller and to generate a configuration file which is used to program the FPGA board.

Keywords: Buck-Boost converter, FPGA, Neuro-Fuzzy Control, VHDL

I. INTRODUCTION

This paper aims to establish the superior performance of neuro fuzzy controllers at various operating points of the buck & boost converters. The basic concept of Neuro-Fuzzy control method is first to use structure-learning algorithm to find appropriate Fuzzy logic rules and then use parameter-learning algorithm to fine-tune the membership function and other parameters. The proposed controller reveals that it is adaptive for all operating conditions. Simulation results are shown and settling time and peak overshoot have been used to measure the performance.

The requirement for short time-to-market has made FPGA devices very popular for the implementation of general purpose electronic devices. Modern FPGA architectures offer the advantage of partial reconfiguration, which allows an algorithm to be partially mapped into a small and fixed FPGA device that can be reconfigured at run time, as the mapped application changes its requirements. Such a feature can be beneficial for modern control applications that may require the change of coefficients, models and control laws with respect to external conditions. The proposed solution is both technically advanced and cost effective, offering flexibility, modularity and efficiency, without performance reduction Traditional frequency domain methods for design of controllers for power converters are based on small signal model of the converter. The small signal model of the converter has restricted validity and changes due to changes in operating point. Also the models are not sufficient to represent systems with strong non-linearity. A state space averaged model of the classical Buck boost DC/DC converters suffers from the well known problem of Right-Half-Plane zero in its control to output transfer function under continuous conduction mode. There are two possible routes to achieve fast dynamic response. One way is to develop a more accurate non-linear model of the converter based on which the controller is designed. The other way is the artificial intelligence way of using human experience in decision-making. Among the various techniques of artificial intelligence, the most popular and widely used technique in control systems is the fuzzy logic. Such an intelligent controller designed may even work well with a system with an approximate model.

II. BACKGROUND

A. Linearized Model for Buck Boost Converter

The Buck-Boost converter is a type of step-down and step-up DC-DC converter. Output of the Buck-Boost converter is regulated according to the duty cycle of the PWM input at fixed frequency. When the duty cycle (d) is less than 0.5, the output voltage of converter is lower than the input voltage. On other condition, when the duty cycle is more than 0.5 the

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output voltage of converter is higher than the input voltage. The basic circuit of a Buck-Boost converter is illustrated in Fig.1 where ***V1*** is input voltage source, ***Vo*** is output voltage, ***SW*** is switching component, ***d*** is diode, ***C*** is capacitance, ***L*** is inductor windings and ***R*** is load resistance..

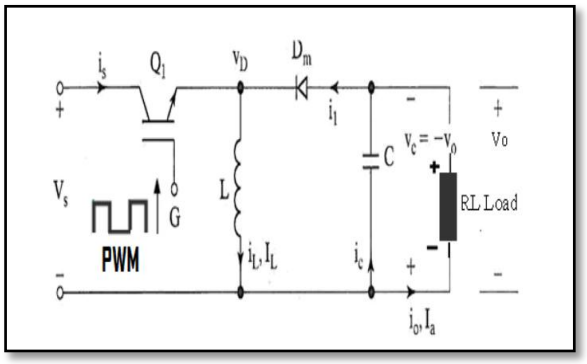

Figure 1: Buck Boost Converter

The equivalent equations for Buck-Boost converter during switching-on can be derived as follow: When the switch is ON, the diode is open

$$v_l = v_S \tag{1}$$

$$v_l = L\left(\frac{di_l}{dt}\right) \tag{2}$$

Substitions of (1) and (2)

$$v_S = L\left(\frac{di_l}{dt}\right) \tag{3}$$

$$\Delta i_{l(\,close\,)} = \frac{v_S DT}{L} \tag{4}$$

When the switch is OFF, the diode is closed

$$v_l = v_0 \tag{5}$$

$$v_L = L\left(\frac{di_l}{dt}\right) \tag{6}$$

Substitutions of (5) and (6)

$$L\left(\frac{di_l}{dt}\right) = v_o \tag{7}$$

$$\Delta i_{l(open)} = \frac{-v_o(1-D)T}{L} \tag{8}$$

Where D is duty cycle.

In steady state operation by solving the linear equation during turn-on and turn-off the average output voltage is derived as follow

$$\Delta i_{l(\,open\,)} + \Delta i_{l(close)} = 0$$

$$\frac{v_S DT}{L} + \frac{v_O(1-D)T}{L} = 0$$

$$\frac{v_O(1-D)T}{L} = \frac{-v_S DT}{L}$$

$$v_O = -v_S \frac{D}{1-D} \tag{9}$$

To develop a dynamic model of the Buck-Boost converter, a state space averaging model is applied. In this method the averaging state space formula of the converter during turn-on and turn-off with D'=1-D where d is duty cycle are given as

$$\dot{X} = AX + BU \tag{10}$$

$$Y = CX \tag{11}$$

where

$$X = \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

$$U = v_1$$

$$Y = v_o$$

$$A = \begin{bmatrix} 0 & \frac{D'}{L} \\ \frac{-D'}{C} & \frac{-1}{RC} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C = [0 \quad 1]$$

The transfer function of the Buck-Boost converter in the continuous system is finally found as

$$G(s) = \frac{-D'R}{LRCs^2 + Ls + D'^2 R}$$

B. Neuro Fuzzy Design procedure:

The design of Neuro Fuzzy controller needs a good

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knowledge of the system operation. The various steps involved in the design of Neuro Fuzzy controller for power converter are stated below. A universal Sugeno type Neuro Fuzzy controller has been simulated for the buck converter.

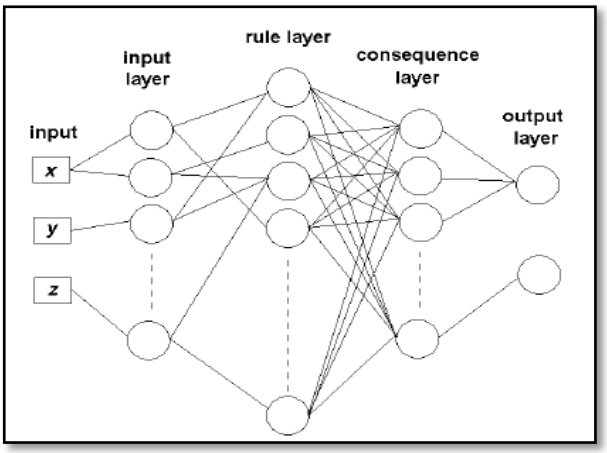

Figure 2: Stucture of Designed NeuroFuzzy

1. *Identification of inputs and outputs:*
This step in the design identifies the key inputs that affect the system performance. The goal of the designer is to ensure that the output voltage matches the reference voltage. The inputs to the Neuro Fuzzy controller are
i. The voltage error.
ii. The change of voltage error.
Some controllers even may use more information in the form of inductor current. The voltage error input is sampled once in every cycle. The output of the controller is the incremental control action i.e. the incremental duty ratio.

2. Fuzzifying the inputs and outputs:
The universe of discourse of the inputs is divided into seven fuzzy sets of triangular shapes. Outputs are also mapped into several fuzzy regions of several singletons.

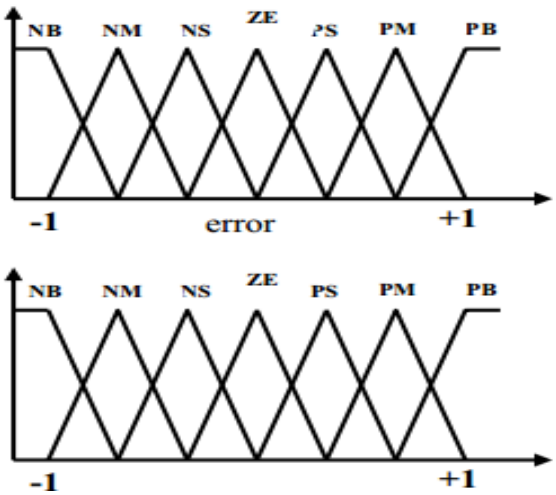

Figure 3: Membership Function

3. Development of rule base:
The rules connecting the inputs and the output singletons are based on the understanding of the system. Normally the fuzzy rules have if…then… structure. The inputs are combined by AND operator. The rule-base contains the fuzzy IF-THEN rules of sugeno's first order type.

4. *Defuzzification:*
The fuzzy conclusion values are mapped to crisp outputs .The output space with the singletons is 'defuzzified' to get a final crisp value of the incremental control, in which the output of each rule is a linear combination of input variables plus a constant term.

C. FPGA

A field programmable gate array (FPGA) is a logic device that contains a two-dimensional array of generic logic cells and programmable switches that can realize any digital system with low cost and reduced time. The FPGA consists of three major configurable elements

1) Configurable Logic Block (CLBs) arranged in an array that provides the functional elements and implements most of the logic in an FPGA. Each logic block has two flip flops and it can realize any 5-input combination logic function.

2) Programmable Interconnect Resources (PIRs) that provides a routing path to connect between the rows and columns of CLBs, and between CLBs and input-output blocks.

3) Input-Output Blocks (IOBs) that provide the interface between the package pins and internal signal lines. It can be configured as an input, output or bidirectional port. The CLBs, IOBs and their interconnectors are controlled by a configuration program store in a chip memory.

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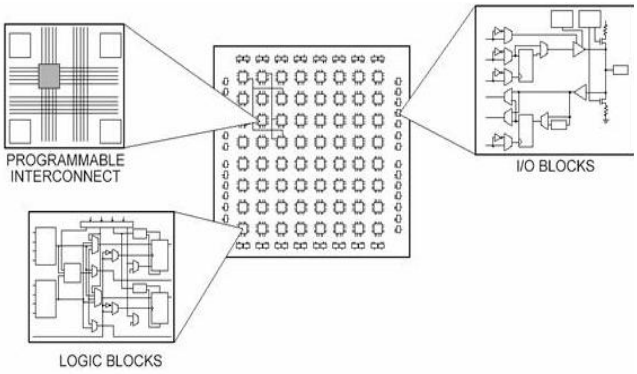
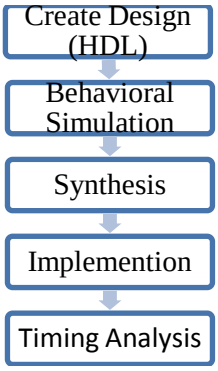


Figure 4: Architecture of FPGA



Figuure 5: Flow chat of FPGA

FPGA Process:

1. Architecture design. This stage involves analysis of the project requirements, problem decomposition and functional simulation (if applicable). The output of this stage is a document which describes the future device architecture, structural blocks, their functions and interfaces.

2. HDL design entry. The device is described in a formal hardware description language (HDL). The most common HDLs are VHDL and Verilog.

3. Behavioral simulation. **:** The simulator software verifies the functionality and timing of your design or portion of your design. The simulator interprets VHDL or Verilog code into circuit functionality and displays logical results of the described HDL to determine correct circuit operation. Simulation allows you to create and verify complex functions in a relatively small amount of time.

4. Synthesis. During synthesis, the synthesis engine compiles the design to transform HDL sources into an architecture-specific design net list. Synthesis decreases design time by eliminating the need to define every gate. During HDL synthesis, XST analyzes the HDL code and attempts to infer specific design building blocks or macros (such as MUXs, RAMs, adders, and subtractors) for which it can create efficient technology implementations.

5. Implementation. After synthesis, you run design implementation, which converts the logical design into a physical file format that can be downloaded to the selected target device.

6. Timing analysis. During the timing analysis special software checks whether the implemented design satisfies timing constraints (such as clock frequency) specified by the user.

D. Proposed block Diagram

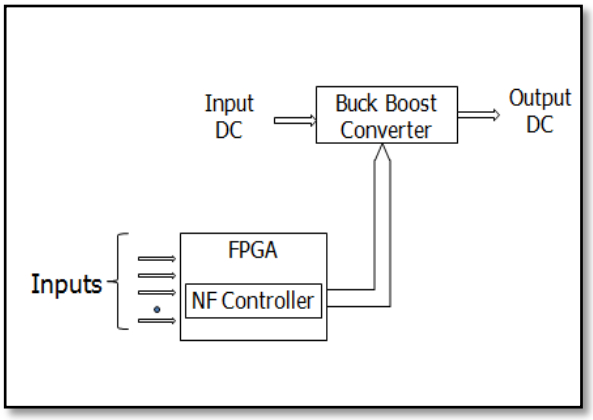


Figure 6: Block Diagram of Project

Figure shows the proposed hardware behavior of neuro fuzzy logic control that will be design VHDL language & implement on Xilinx Spartan 3E FPGA board. First, a VHDL codes are downloaded from the host computer into the FPGA chip using a USB cable. Then, Edge connector is used to interface the board (NF controller) with model of the buck boost converter. The digital input with switches has been applied as input data to the FPGA boards. The FPGA board generates the digital inputs to the NF controller. The NF controller generates a suitable digital control signal based on the rules that were stored in the FPGA chip. The digital control signals generate pulse waveform and pulse waveform will be applied as an input to the buck boost converter. At the same time buck boost converter also get DC input supply. Thus at the output we get DC output.

III. CONCLUSION

The buck boost converters are subjected to various disturbances of input voltage and load changes is performed to demonstrate the effectiveness of the

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proposed controller. The conclusions drawn from the results are

I. The proposed novel controller gives small overshoots and has much superior performance compared to the local PI controllers.

II. The Neuro-Fuzzy controller behaves effectively like an adaptive local tuned controller designed for each operating point and gives an improved performance compared to the conventional PI controller.

III. The proposed Neuro-Fuzzy controller is adaptive for all the operating point as compared to Fuzzy controller.

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