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Simulation Modelling on Space Vector Modulated Quasi Z-Source Inverter Fed PMSM

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Abstract: A three level inverters with single quasi z-source fed PMSM motor drive is proposed in this project .The proposed inverter has the main features in that the output voltage can be bucked or boosted and in-phase with the input voltage. The quasi z-source concept can be applied to all dc-ac, ac-dc and dc-dc power conversion whether two-level or multi-level. The input voltage and output voltage share the common ground, the size of the inverter is reduced, and it operates in a continuous current mode. This paper presents control of a quasi z-source neutral point clamped inverter using the space vector modulation technique. The operating principles and a steady state analysis are presented .The simulation results verified that the inverter has the lower input current harmonics distortion, a high efficiency, as it makes possible to avoid voltage spikes on the switches.

Index terms: Buck-Boost, Neutral Point Clamped (NPC) Inverter, Space Vector Modulation (SVM), Quasi Z-Sour Inverter.

I.INTRODUCTION

Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter, the diode clamped inverter, and the capacitor clamped inverter. Among the three, the three level diode clamped [also known as the neutral point clamped (NPC)] inverter has become an established topology in medium voltage drives and is arguably the most popular certainly for three-level circuits. However, the NPC inverter is constrained by its inability to produce an output line-to-line voltage greater than the dc source voltage. For applications where the dc source is not always constant, such as a fuel cell, Photo voltaic array, and during voltage sags, etc., a dc/dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favorably located. This increases the system complexity and is desirable to eliminate if possible. The quasi Z-source inverter topology was proposed to overcome the above limitations in traditional inverters. The quasi z-source concept can be applied to all dc-to-ac , ac-to-dc , ac-to ac , and dc-to-dc , power conversion whether two-level or multilevel. The quasi z-source concept was extended to the NPC inverter, where two additional quasi z-source networks were connected between two isolated dc sources and a traditional NPC inverter. In spite of its effectiveness in achieving voltage buck–boost conversion, the quasi z-source NPC. To overcome the cost and modulator complexity issues, the design and control of an NPC inverter using a single quasi z-source network was presented in. The operational analysis and optimal control of the Reduced Element Count (REC) quasi z-source NPC inverter was subsequently described in. The REC quasi z-source NPC inverter is expected to find applications in grid connected Distributed Generation (DG) systems based on renewable energy sources such as photovoltaic systems, wind turbines, and fuel cell stacks. The power quality of current injected to the grid is improved because of the three-level structure. It can also find use in adjustable speed drive systems in applications such as conveyor belts, fans, and water pumps. In, the modulation of the REC quasi z-source NPC inverter was described using the carrier-based approach. However, the space vector modulation (SVM) approach offers better harmonic performance (compared with carrier-based pulse width modulation (PWM) strategy without zero-sequence voltage injection) and can more conveniently handle overall switching patterns and constraints, and it is simple to implement using a DSP. The contribution of this paper is, therefore, the development of a modified SVM algorithm for controlling the REC quasi z-source NPC inverter. And simulations results are used to verify the operation of the circuit and proposed SVM-based modulation. It has recently been demonstrated that the space vector modulation can be implemented on traditional two-level converters using a classification technique. The classification algorithm requires less computational effort, and as a result, less computational time, when compared with the conventional SVM methods. The technique does not compromise accuracy, and guarantees exact positioning of the switching instants. Software complexity of the SVM increases significantly with the number of converter levels. Also, more non-linear function approximation and therefore less accurate positioning of switching instants occur as the number of converter levels increase.

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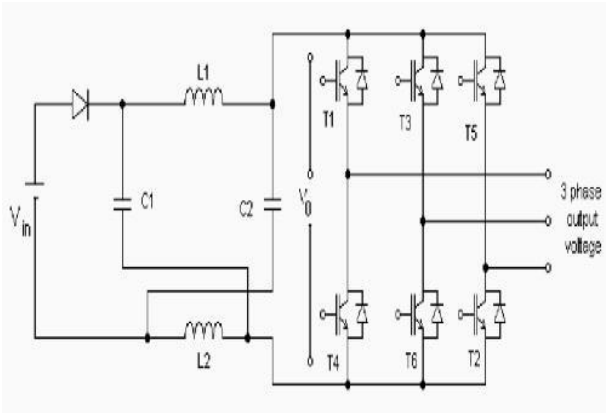

Fig.1. topology of two level quasi z-source inverter

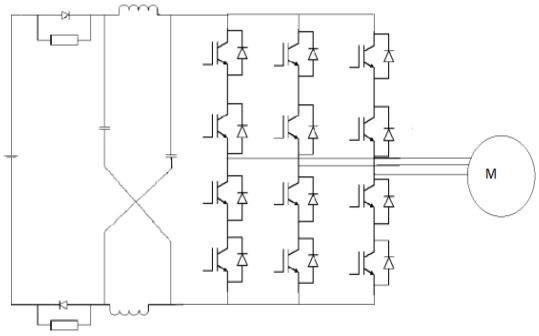

Fig.2. topology of an REC quasi z- source NPC inverter

II. REVIEW OF QUASI Z-SOURCE CONCEPT:

The topology of a two-level quasi z-source inverter is shown in Fig. 1. The only difference between the z-source inverter and a traditional voltage source inverter (VSI) is the presence of a quasi z-source network comprising a split-inductor (*L*1 and *L*2) and two capacitors (*C*1 and *C*2). The unique feature of the two-level quasi z-source inverter is that the output ac voltage fundamental can be controlled to be any value between zero and (theoretically) infinity regardless of the dc source voltage. Thus, the quasi z-source inverter is a buck–boost inverter that has a very wide range of obtainable output voltage. Traditional VSI cannot provide such features. In Fig. 1, the two-level quasi z-source inverter bridge has 15 permissible switching states unlike the traditional two-level VSI that has 8. The traditional three-phase VSI has six active states when the dc voltage is impressed across the load and two zero states when the load terminals are shorted through either the lower or upper three devices, respectively.

However, the two-level Quasi z-source inverter bridge has seven extra zero states (termed shoot through states) when the load terminals are shorted through both upper and lower devices of any one phase leg (i.e., both devices are gated ON), any two phase legs, or all three phase legs. These shoot-through states are forbidden in a traditional VSI for obvious reasons. The Quasi z-source network makes the shoot-through zero states possible and provides the means by which boosting operation can be obtained. Critically, any of the shoot-through states can be substituted for normal zero states without affecting the PWM pattern seen by the load. Therefore, for a fixed switching cycle, Instead, with the shoot-through states inserted, the effective inverter dc link voltage *Vi* can be stepped up as given in (1) Consequently, taking also the PWM modulation index *M* into account, the phase ac output voltage *Va* ($x_E\{a, b, c\}$) can be expressed by (2)

$$V_i = \frac{E}{1-\frac{2.T_{ST}}{T}} = B.E, B \geq 1 \qquad (1)$$

$$V_x = \frac{M.V_i}{\sqrt{3}} = B.\{\frac{ME}{\sqrt{3}}\} \qquad (2)$$

Where TST and T are the shoot-through interval and switching period, respectively, B is the boost factor and the term in parenthesis represents the phase ac output voltage of a traditional VSI. Equations (1) and (2) show that the ac output voltage of a Quasi Z-source inverter can be regulated from zero to the normal maximum by altering M and maintaining
B = 1, or can be boosted above that obtainable with a traditional VSI by choosing B > 1.

III. TOPOLOGY OF REC QUASI Z-SOURCE INVERTER:

A .Extension Of The Quasi Z-Source Concept To The NPC Inverter

To describe the operating principle of the REC Z-source NPC inverter shown in Fig. 2, we concentrate initially on the operation of one phase leg. The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Switching state “P” denotes that the upper two switches in a phase leg are gated ON, “N” indicates that the lower two switches conduct, and “O” signifies that the inner two switches are gated ON. However, each phase leg of the Z-source NPC inverter has three extra switching states which resemble the “O” state of the traditional NPC inverter.

These extra switching states occur when all the four switches in any phase leg are gated ON [full-shoot-through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower shoot-through (LST)].

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TABLE I
SWITCHING STATES OF AN REC QUASI Z-SOURCE INVERTER

State type	ON switches	ON diodes	V_{xo}	Switching state
NST	QX1,QX2	D1.D2	$+\frac{V_i}{2}$	P
NST	QX2	D1,D2, {DX1 or DX2}	0	O
NST	QX'1	D1,D2	$-\frac{V_i}{2}$	N
FST	QX1,2	-----	0	FST
UST	QX1,2	DX2,D1	0	UST
LST	QX2,QX'1, 2	DX1,D2	0	LST

B. Circuit Analysis

Among the three-level Quasi Z-source power converter topologies reported to date, the Quasi Z-source NPC inverter implemented using a single *LC* impedance network (see Fig. 2) is considered to be an optimized topology in terms of component count. Referring to Fig. 2, the REC Quasi Z-source NPC inverter is supplied with a split dc source. The middle point *O* is taken as a reference. By controlling the switches of each phase leg according to the combinations presented in Table I, each output phase voltage $Vxo(x_E\{a, b, c\})$ has three possibilities: *Vi*/2, 0, and −*Vi*/2. When the REC Quasi Z-source NPC inverter is operated without any shoot-through states, then *Vi* is equivalent to 2E. As noted earlier, with this kind of operation, the maximum obtainable output line-to-line voltage cannot exceed the available dc source voltage (2E). Therefore, to obtain an output line-to-line voltage greater than 2E, shoot-through states are carefully inserted into selected phase legs to boost the input voltage to *Vi* > 2E before it is inverted by the NPC circuitry. Thus, the REC Quasi Z-source inverter can boost and buck the output line-to-line voltage with a single-stage structure. In, two new switching states namely the UST and LST states were identified, in addition to the FST state and the non shoot-through (NST) states (P, O, and N) that had been reported earlier in. Although operation using the FST and NST states is possible (termed the FST operating mode), it is generally preferable to use the UST and LST states in place of the FST states (termed the ULST operating mode).

The ULST operating mode is preferred because it produces an output voltage with enhanced waveform quality. The simplest FST operating mode requires all four switches in a phase leg (see Table I) to be turned ON. This is not a minimal loss approach since, for example, switching phase A from +E through FST to 0 V would require switches *{*Qa1, Qa2, Qa'1, Qa'2*}* changing from *{*ON, ON, OFF, OFF*}* through *{*ON, ON, ON, ON*}* to *{*OFF, ON, ON, OFF*}*. An alternative FST operating mode which gives minimal loss uses two phase legs to create the shoot-through path. This requires, however, the output line-to-line voltage obtained using the minimal loss FST approach has higher harmonic distortion (compared to the ULST approach) in its output voltage waveform because the voltage levels produced do not have adjacent level switching. Therefore, in this paper, the ULST operating mode is used for controlling the REC Quasi Z-source NPC inverter. Fig. 3(a) shows the simplified equivalent circuit for the NST state, while Fig. 3(b) and (c) shows the UST and LST states. Note that there are multiple ways of creating the UST and LST states using different phases. The choice between these is discussed later. Assuming that the Z-source network is symmetrical (*L*1 = *L*2 = *L* and *C*1 = *C*2 = *C*), then *VL*1 = *VL*2 = *VL* and *VC*1 = *VC*2 = *VC* and the voltage expressions for the NST state are as follows:

NST

$$VL = 2E - VC \quad (3)$$

$$VP = +Vi/2, \quad VN = -Vi/2 \quad (4)$$

$$VI = 2(VC - E) \quad (5)$$

Similarly, the voltage expressions for the UST and LST states are as follows:

UST

$$VL1 = E \quad (6)$$

$$VP = 0\ V,\ VN = E - VC1 \quad (7)$$

LST

$$VL2 = E \quad (8)$$

$$VP = -E + VC2,\ VN = 0\ V \quad (9)$$

We denote the duration of the NST, UST, and LST states by T_N, T_U, and T_L, respectively, and the switching period by *T*. Also, we assume that *TU* and *TL* are equal (this is necessary to ensure symmetrical operation) and denote the total combined UST and LST duration by *T*ULST.

At steady state, the average voltage across the inductors is zero; therefore, averaging the inductor voltage over one switching period, we have

$$\frac{(2E - V_C).T_N + E.T_U + E.T_L}{T} = 0 \quad (10)$$

$$T_N + T_U + T_L = T \quad (11)$$

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TABLE 2

SWITCHING COMBINATION AND SWITCHING STATES FOR A THREE LEVEL INVERTER (1 PHASE LEG)

S_{1X}	ON	OFF	OFF
S_{2X}	ON	ON	OFF
S_{3X}	OFF	ON	ON
S_{4X}	OFF	OFF	ON
V_{XO}	$V_{DC}/2$	0	$-V_{DC}/2$
Switching state	**P**	**O**	**N**

Solving for *VC* using (10) and (11), we have

$$V_C = 2E.\{\frac{1-\frac{T_{ULST}}{2T}}{1-\frac{T_{ULST}}{T}}\}(12)$$

Substituting (12) into (5), we have the dc-link voltage *Vi* during the NST state as

$$v_{i-NST}=\{\frac{2E}{1-\frac{T_{UST}}{T}}\}(13)$$

Similarly, when (12) is substituted into (7) and (9) and noting that Vi = VP − VN , we have the dc-link voltage during the UST and LST states as

$$V_{i-UST} = v_{i-LST} = \{\frac{E}{1-\frac{T_{ULST}}{T}}\}(14)$$

It is noted from (13) and (14) that the higher dc-link voltage is present during the NST states and it is twice the dc-link voltage available during the UST and LST states, as required.

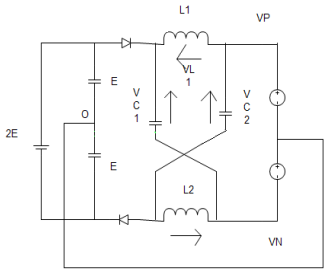

Fig 3(a) NST

The fundamental peak ac output voltage *Vxo* ($x_E\{a, b, c\}$) is given by

$$V_{xo} = \frac{M}{\sqrt{3}}.V_{i-NST}(15)$$

$$V_{xo} = (\frac{1}{1-\frac{T_{ULST}}{T}})\{\frac{M}{\sqrt{3}}(2E)\} = B^{'}\{\frac{M}{\sqrt{3}}(2E)\}(16)$$

Where $B \geq 1$ is the boost factor and all the other symbols have their usual meaning.

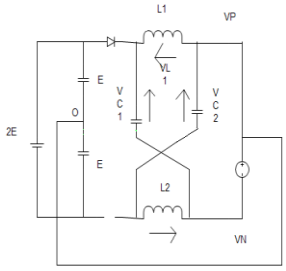

Fig 3(b) UST

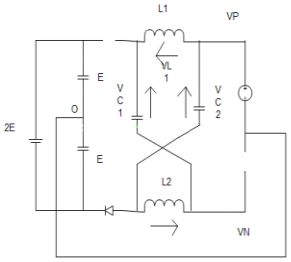

Fig 3(c) LST

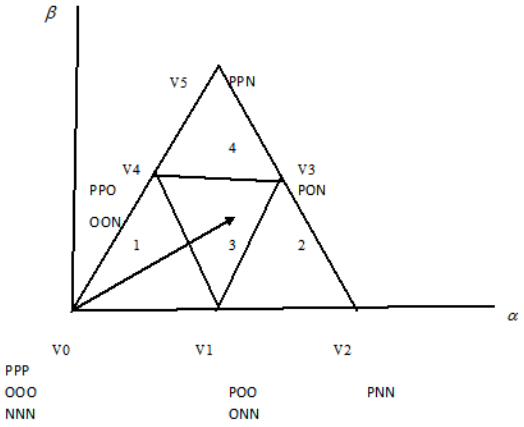

Fig 4. Space vector diagram of sector 1 for a three-level inverter

1V. MODIFIED SVM OF THE REC QUASI Z-SOURCE NPC INVERTER

A.Duty Cycle Calculation

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The space vector diagram of a traditional NPC inverter for sector 1 is shown in Fig. 4. The reference vector $\vec{V}_{ref}$ can be expressed as

$$V_{ref}(t)=\frac{2}{3}[v_{ao}(t)e^{j0}+v_{bo}(t)e^{\frac{j2\pi}{3}}+v_{co}(t)e^{\frac{j4\pi}{3}}](17)$$

$$d_1.\vec{V}_1+d_2.\vec{V}_7+d_3.\vec{V}_{13}=\vec{V}_{ref}$$

$$d_1+d_2+d_3=1(18)$$

$$\vec{V}_1=\frac{1}{3}.(2E)$$

$$\vec{V}_7=\frac{\sqrt{3}}{3}.e^{\frac{j\pi}{6}}.(2E)$$

$$\vec{V}_{13}=\frac{2}{3}.(2E)$$

$$\vec{V}_{ref}=V_{ref}.e^{j\theta} \quad (19)$$

Substituting (19) into (18), the duty ratios of the nearest three voltage vectors are given by (20), where *M* is the modulation index and $0 \le \theta \le \pi/3$

$$d_1=2-2M\sin(\frac{\pi}{3}+\theta)$$

$$d_2=2M\sin\theta$$

$$d_3=2M\sin(\frac{\pi}{3}-\theta)-1(20)$$

A similar procedure is used for calculating the duty ratios of the selected voltage vectors in all the other triangles. To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence. Ideally, a switching sequence is formed in such a way that a high quality output waveform is obtained with minimum number of switching transitions.

V. SIMULATION RESULTS

To verify the proposed approach, simulations were first performed in SABER before the proposed SVM-based modulation algorithm was validated simulated using an REC Quasi Z-source NPC inverter prototype. These errors are due to the fact that the voltage drop across the diodes D1, D2 and the inductors L1, L2 was neglected in the derivation of all the equations. The simulation results show that the REC Z-source NPC inverter, with the proposed SVM algorithm, is able to boost the output line-to-line voltage to a value higher than the available dc supply voltage with sinusoidal output currents. Finally, the simulation results of the space vector modulation described in using the same parameters as those of the proposed SVM strategy, and the total harmonic distortion (THD) of the output line-to-line voltage is compared to that of the proposed SVM strategy. It can be concluded that the harmonic performance of the proposed SVM strategy is comparable to the carrier-based PWM with zero-sequence voltage injection.

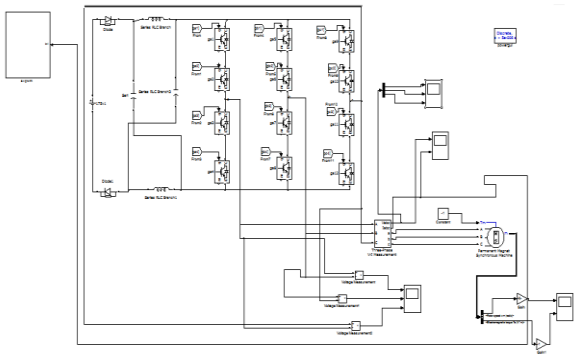

Fig 4.simulation diagram for space vector modulated quasi z-source inverter fed PMSM

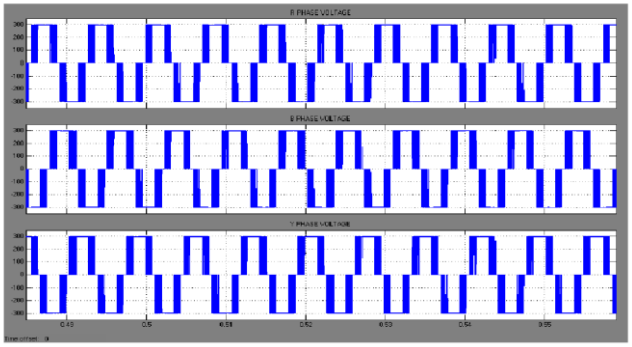

Fig 5. space vector modulated quasi z-source inverter fed PMSM simulated 3phase output

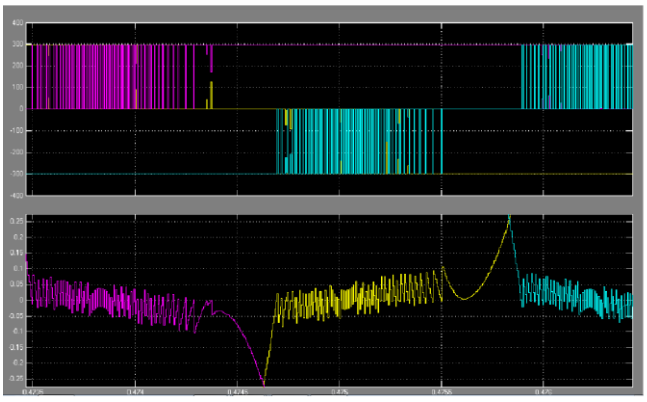

Fig 6.voltage and current for space vector modulated quasi z- source inverter fed PMSM

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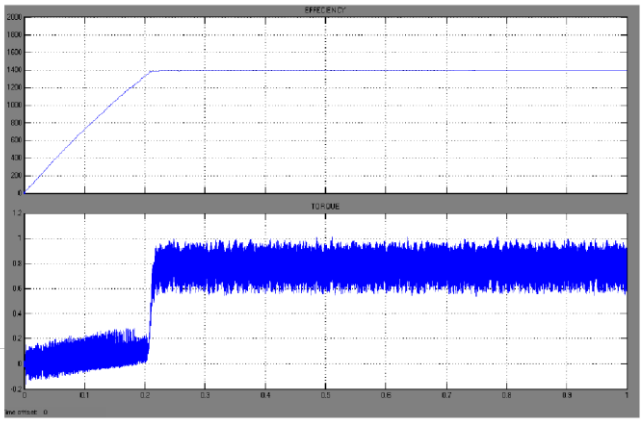

Fig 7.motor output for space vector modulated quasi z-source inverter fed PMSM

V CONCLUSION

A modified SVM for an REC Quasi Z-source NPC inverter with PMSM drive is presented. Using carefully inserted UST and LST states to the traditional NPC inverter state sequence, the REC Quasi Z-Source NPC inverter functions with the correct volt–second average and voltage boosting capability regardless of the angular position of the reference vector. The insertion of the shoot through states was such that the number of device commutations was kept at a minimum of six per sampling period, similar to that needed by a traditional NPC inverter. The presented concepts have been verified in simulations. In addition, the modified single quasi z-source network has the unique advantages in that the size of the inverter is reduced and the operation of the input current is continuous, with additional features, such as reduction in the in-rush, a harmonic current, and an improved power factor.

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