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SPARSE MATRIX CONVERTER FED INDUCTION DRIVE USING FUZZY LOGIC CONTROLLER

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Abstract: In this project, quasi network based sparse matrix converter and a compensation method based on a fuzzy logic controller to compensate the input voltage. The structure of an SMC to reduce the number of unipolar power semiconductor switches employs a quasi network to overcome the inherent limitation of the low voltage transfer ratio of conventional matrix converters. Although the SMC is a two-stage converter, it directly connects between a source and a load through a quasi network, which is designed to have smaller passive components as the only purpose is voltage boosting. The operational principle of the SMC is described and its modulation strategy is explained. Simulation results are shown to verify the feasibility of the SMC and its operation.

Index Terms: Sparse Matrix Converter, Quasi Network, Compensation, Fuzzy Logic Control.

I.INTRODUCTION

Matrix converter is capable of direct conversion from AC to AC by using bidirectional fully controlled switches. In ac-ac power conversion, two types of conversion systems are used. They are ac-dc-ac two stage conversion system and the other is an ac-ac-ac one stage direct conversion system. The traditional indirect converter produces variable-amplitude and/or frequency output voltages with a stiff dc-link voltage that is acquired by a larger dc-link energy-storage component, such as an electrolytic capacitor. Unlike the traditional indirect converter, the direct converter connects any input phase to any output phase with an array of controlled power semiconductor switches without the dc-link energy-storage component. This type of converter is called as matrix converter[1].

The matrix converters can be implemented with two different topologies: one is a direct matrix converter and the other is an indirect matrix converter shown in Fig. 1. The structure of the direct matrix converter is based on direct ac–ac power conversion by coupling the input and output sides with nine bidirectional switches, while the indirect matrix converter is based on ac–dc–ac power conversion without any dc-link energy-storage component[2]. Although the direct and indirect matrix converters differ with respect to the circuit configuration, control strategy, efficiency, and complexity, they provide similar basic functionalities, such as sinusoidal input currents and bidirectional power flow with the same number of unipolar power semiconductor switches[3]. Since a matrix converter connects a source and a load without any energy-storage component, its output voltage can only be synthesized directly with input line-to-line voltages. Under this restriction, the maximum output voltage that the matrix converter can produce without entering the over modulation range is equal to 86% of the maximum input voltage.

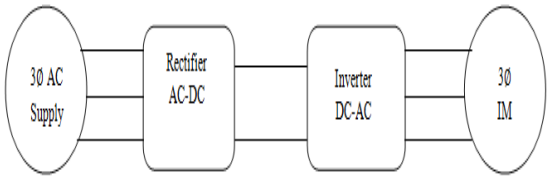

Fig. 1. Matrix converter

For electrical drive applications, it means that a derated motor or a nonstandard motor is required. Furthermore, disturbances at the input source are immediately reflected to the load. The unbalanced input voltages can result in unwanted output harmonic currents and the short-time input-voltage sag can bring the voltage sag on the load. These can deteriorate the performance of the load[3]-[5],[12]-[22].

II. QUASI NETWORK

The quasi z-source inverter (QZSI) is a single stage power converter derived from the Z-source inverter topology, employing a unique impedance network. The conventional VSI and CSI suffer from the limitation that triggering two switches in the same leg or phase leads to a source short and in addition, the maximum obtainable output voltage cannot exceed the dc input, since they are buck converters and can produce a voltage lower than the dc input voltage. Both Z-source inverters and quasi-Z-source inverters overcome these drawbacks, by utilizing several shoot-through zero states. A zero state is produced when the upper three or lower three switches are fired simultaneously to boost the output voltage. Sustaining the

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six permissible active switching states of a VSI, the zero states can be partially or completely replaced by the shoot through states depending upon the voltage boost requirement. Quasi-Z-source inverters (QZSI) acquire all the advantages of traditional Z-source inverter. The impedance network couples the source and the inverter to achieve voltage boost and inversion in a single stage. By using this new topology, the inverter draws a constant current from the PV array and is capable of handling a wide input voltage range. It also features lower component ratings, reduces switching ripples to the PV panels, causes less EMI problems and reduced source stress compared to the traditional ZSI.

The QZSI circuit differs from that of a conventional ZSI in the LC impedance network interface between the source and inverter. The unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state which is forbidden in traditional VSI. This network will effectively protect the circuit from damage when the shoot through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage. The Quasi network consists of inductors and capacitors connected as shown in fig. This network is employed to provide an impedance source, coupling the converter to the load. The dc source can be a battery, diode rectifier, thyristor converter or PV array. The QZSI topology is shown in the Fig. 2.

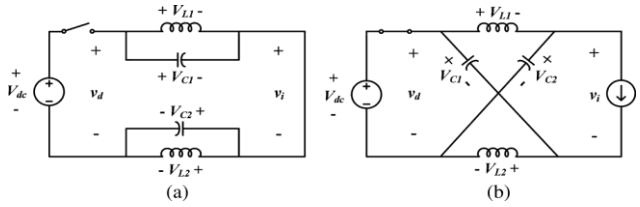

Fig. 2. Equivalent circuit of the quasi Z-source inverter
(a) Shoot through state mode (b) Nonshoot-through state mode

A. OPERATION

The ZSMC mainly operates in two different operating modes one is a shoot-through state mode, in which the energy is charged in the Z-source network, and the other is a non shoot-through state mode (or a normal operating mode), in which the stored energy is used to synthesize the output voltages. If it is assumed that the Z-source inverter is fed by a constant dc-link voltage during one switching period, two equivalent circuits for each of these operating mode During the shoot-through state mode *T0 , the Z-source inverter* stage is intentionally short circuited and the dc-link switch S1 is opened, which separates the dc-link from the rectifier stage. During this period, the rectification stage performs the commutation as mentioned earlier. The shoot through can be achieved in seven different ways: short circuit of any one phase leg, any two phase legs, or all three phase legs. This produces a shoot through zero state in which the energy is charged in the Z-source network. During the non shoot-through state mode *T1 , the Z-source* inverter operates as a normal inverter and the dc-link switch S1 is closed, which will allow the bidirectional flow of the dc-link current.

B. RECTIFIER STAGE

In order to ensure proper operation of the ZSMC, a dc-link voltage should always be positive and the bidirectional current flow capability of the rectifier stage should be achieved by using bidirectional switches. The rectifier stage of the ZSMC can commutate with zero dc-link current when the Z-source inverter is in the shoot-through zero state. Therefore, the rectifier stage has only to ensure that no short circuit of an input line-to-line voltage occurs. In order to make a maximum dc-link voltage available to form the output voltage, the input phase with the highest absolute value is clamped to the positive or negative dc-link bus voltage according to its polarity.

C. INVERTER STAGE

A modified SVPWM algorithm with a shoot-through capability can be used for the Z-source inverter stage, In order to ensure zero-current switching in the rectifier stage, the inverter is switched into the shoot-through zero state, and then, the rectifier stage commutates with zero current. The shoot-through zero state can be inserted in the middle of a free-wheeling state (zero vector).

It should be noted that each phase leg switches ON and OFF two times per switching period without changing the total time of a free-wheeling state. The active states are thereby unchanged. However, the equivalent dc-link voltage to the inverter is boosted by the shoot-through zero state.

D. INDUCTOR DESIGN

During traditional operation mode, the capacitor voltage is always equal to the input voltage. So there is no voltage across the inductor. During shoot through mode, the inductor current increases linearly and the voltage across the inductor is equal to the voltage across the capacitor. The average current through the inductor is given by, IL = P/Vdc (3.11). Where P is the total power and Vdc is the input voltage. The average current at 1kW and 150 V input is IL (avg) = 1000/150 = 6.67A. The maximum current occurs through the inductor when the maximum shoot-through happens, which causes maximum ripple current. In this design, 30% current ripple through the inductors during maximum power operation was chosen. Therefore the allowed ripple current was 4A and maximum current is 10.67A. For a switching frequency of 10 kHz, the average capacitor voltage is VC = (1-TO/T) * Vdc / (1-2TO/T) Substituting the values in the above equation the average capacitor voltage is 300V. So the inductance is L = 0.1 * 10 * 300 / 10.67 = 3mH

E. CAPACITOR DESIGN

The purpose of the capacitor is to absorb the voltage ripple and maintain a fairly constant voltage. During shoot-through the capacitor charges the inductors and the current through the capacitor equals the current in the inductor. Therefore the voltage ripple across the capacitor is VC = IL(avg)TS/C (3.13). The capacitor voltage ripple is 0.17%.

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Substituting the above values in the equation the required capacitance was found to be C = 6.67 * 0.1 * 10 (300 * 0.0017) = 1000μF Hence the impedance network of the Quasi Z-Source inverter consists of a inductor of value 3mH and capacitor of 1000μF.

III. COMPENSATION METHOD BASED ON FLC

Although the ZSMC is a two-stage converter, it directly connects a source and a load with a Z-source network, which is designed to have passive components only for the purpose to boost the output voltage. Therefore, if the input voltages of the ZSMC are unbalanced, the dc-link voltage is directly affected. The output voltages synthesized with the distorted dc-link volt- age are also distorted, which will cause undesirable harmonics in the output currents of the ZSMC. The grid usually suffers the steady state and transient voltage unbalanced problems, which are caused by various factors in the transmission and distribution networks. These problems are difficult to predict and to estimate. An FLC is basically a nonlinear adaptive controller so that it can give robust performance for both linear and nonlinear systems. Therefore, it is attractive in a ZSMC and may have better performance than a traditional PI controller under these distorted and unpredictable conditions. This paper introduces an FLC-based output-current- compensation method.

A.FLC

The FLC is fed by the instantaneous error e of I_o and produces a voltage transfer ratio q for the Z-source inverter. With this voltage transfer ratio, the Z-source inverter can synthesize proper output voltages that will control a constant I_o .The FLC uses the error e and the change of error "ce" as input as shown in Fig. 3. The instantaneous value of the error can be obtained by subtracting a reference current space vector I_{ref} from the measured output current space vector and calculated. The change of error is the difference between the present and previous values of the error. These inputs are converted into per-unit signals by multiplying with the corresponding scaling factors G_e and G_C .With these per-unit input values, a fuzzification process is performed using the triangular membership functions shown in Fig. 4(a). Asymmetrical triangular membership functions have been selected in this design, which causes crowding near the origin and, therefore, gives more precision near the origin. The universe of discourse for input variables *e(pu)* and ce*(pu)* spreads in the region from −1 to +1 and the membership functions are symmetrical on both positive and negative sides. The evaluation of control rules is performed with the rules shown in Table I. The top row and left column describe the sets for the input variables *e(pu)* and ce*(pu)*, respectively. Because there are seven sets for each input variable, there are in total 49 rules in Table I. The defuzzification is carried out using singleton membership functions as shown in Fig. 4(b), which is usually called the zero-order Sugeno method of implication. The output of the FLC system is the change of voltage transfer ratio "cq" and its universe of discourse is between −1 to +1 as well. The actual voltage transfer ratio q can be obtained by integrating the change of voltage gain after multiplying with a proper scaling factor G_q . For a conventional matrix converter, a saturation block is needed for the FLC system because it has the inherent limitation of the voltage transfer ratio with the maximum value. However the Quasi ZSMC can theoretically have any value from zero to infinity as a voltage transfer ratio. Nevertheless, for an actual implementation, the maximum voltage transfer ratio of the Quasi ZSMC is also restricted by the size of the inductors and capacitors in the Z-source network another hardware ratings.

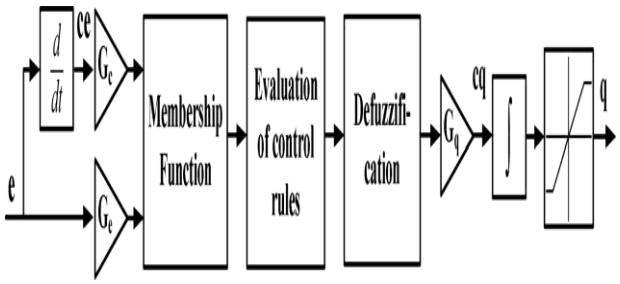

Fig. 3. Block diagram of FLC

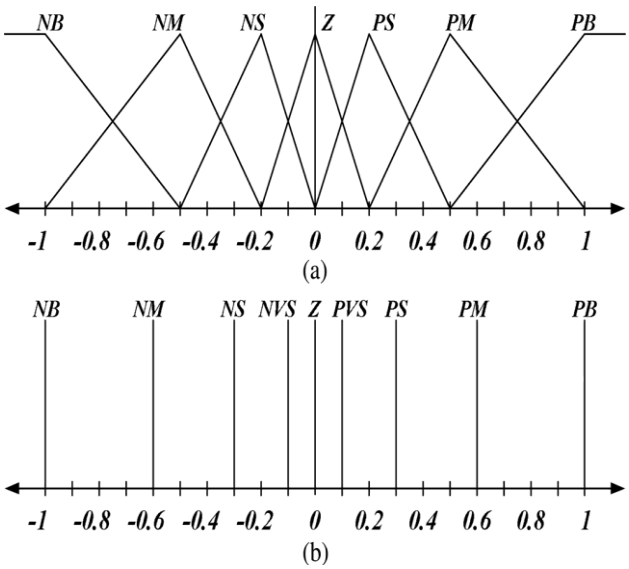

Fig. 4. Membership function for (a) fuzzification (b) defuzzification

IV. SIMULATION

Using MATLAB simulation have been done to verify the output performance of the matrix converter using the compensation method. MATLAB stands for "Matrix Laboratory" and is a numerical computing environment and fourth-generation programming language. Developed by the MathWorks, MATLAB allows matrix multiplications, plotting of functions and data, implementation of algorithms, creation of users interfaces and interfacing with programs written in other languages including C.C++ and Fortran. Although MATLAB is intended primarily for numerical computing, an optional toolbox uses the MuPAD symbolic engine, allowing access

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to symbolic computing capabilities. An additional package, Simulink, adds graphical multi-domain simulation and Model-Based Design for dynamic and embedded systems. In 2004, MATLAB had around one million users across industry and academia. MATLAB users come from various backgrounds of engineering, science, and economics. MATLAB is widely used in academic and research institutions as well as industrial enterprises. Simulations have been done to verify the boosting feature and evaluate the output performance of the ZSMC under unbalanced input-voltage conditions using the proposed compensation method. The simulation circuit of the sparse matrix converter fed induction drive is shown in Fig. 5.and the simulated results are shown in Fig. 6. Furthermore, a current-compensation method based on an FLC has been presented to improve the output performance of the ZSMC. The simulation results confirm the output performance of the ZSMC using the current-compensation method.

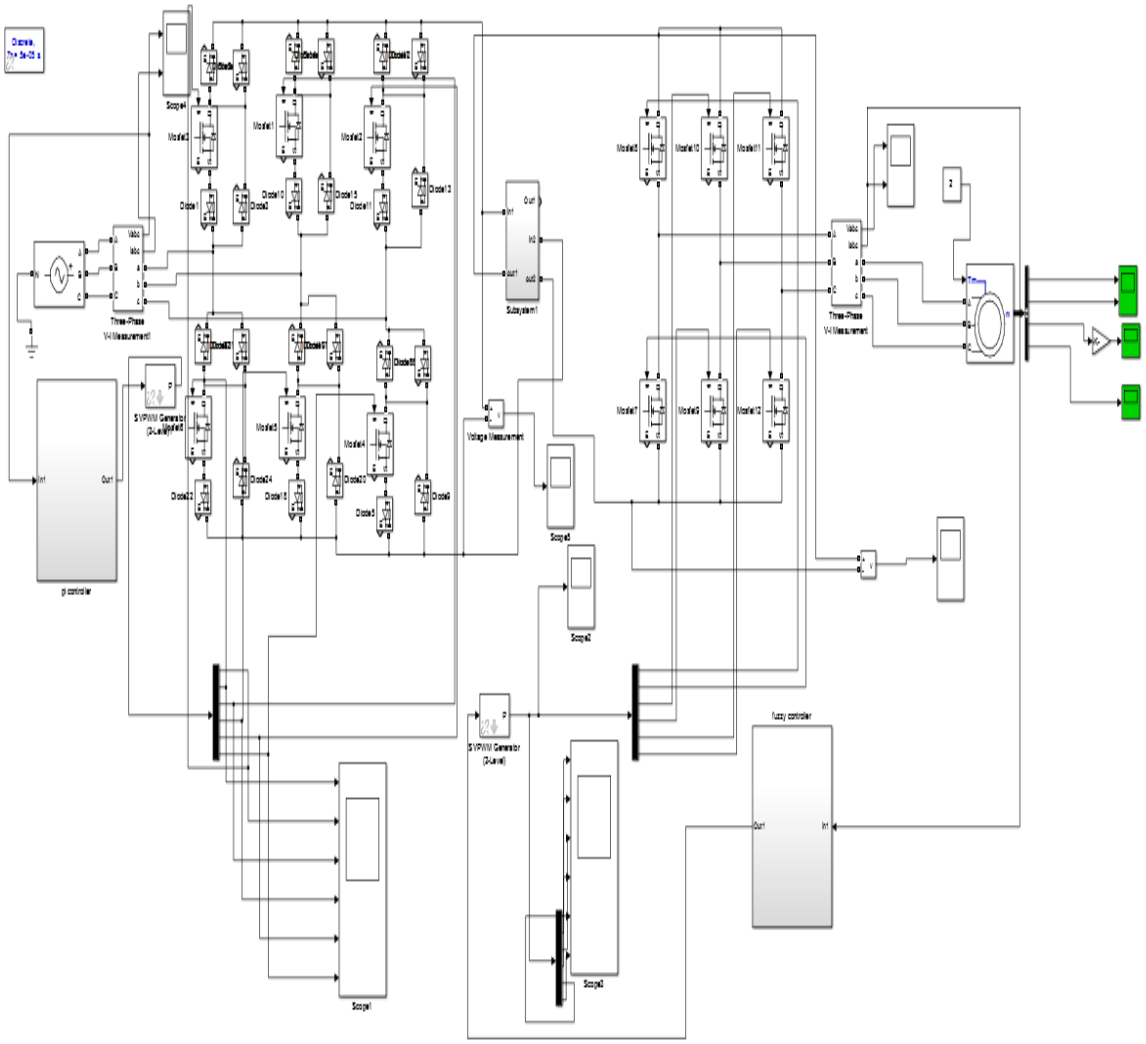
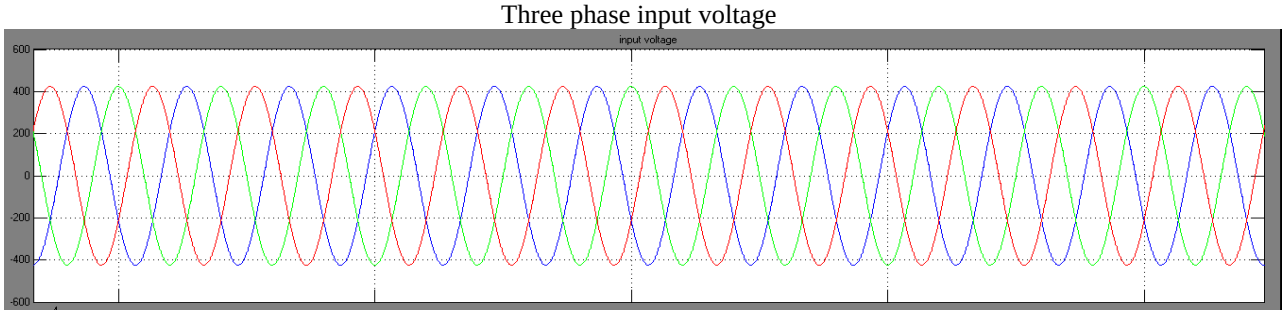


Fig. 5. Simulation circuit for sparse matrix converter fed induction drive



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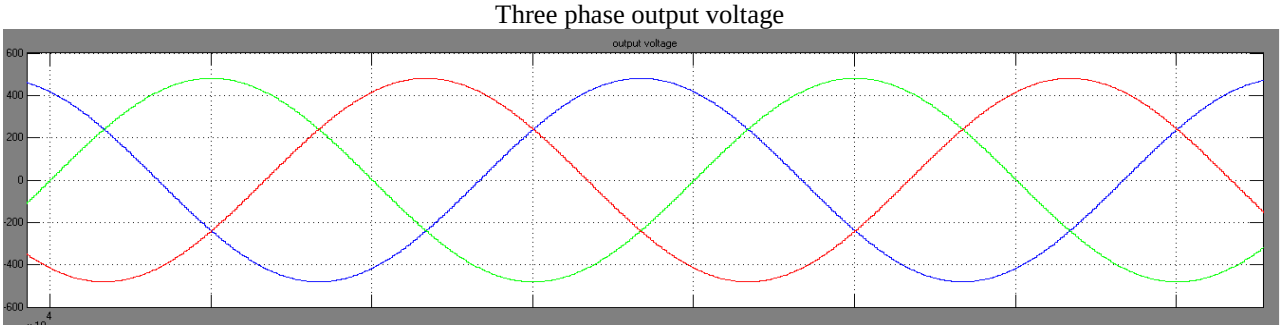
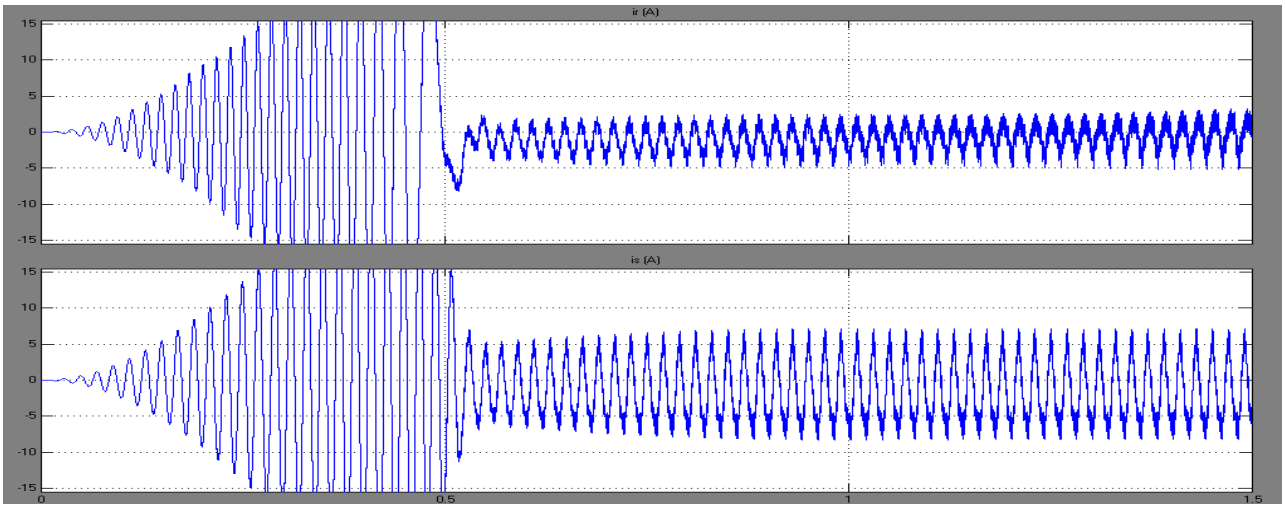
Three phase output voltage



Stator and rotor current of the motor



Motor speed

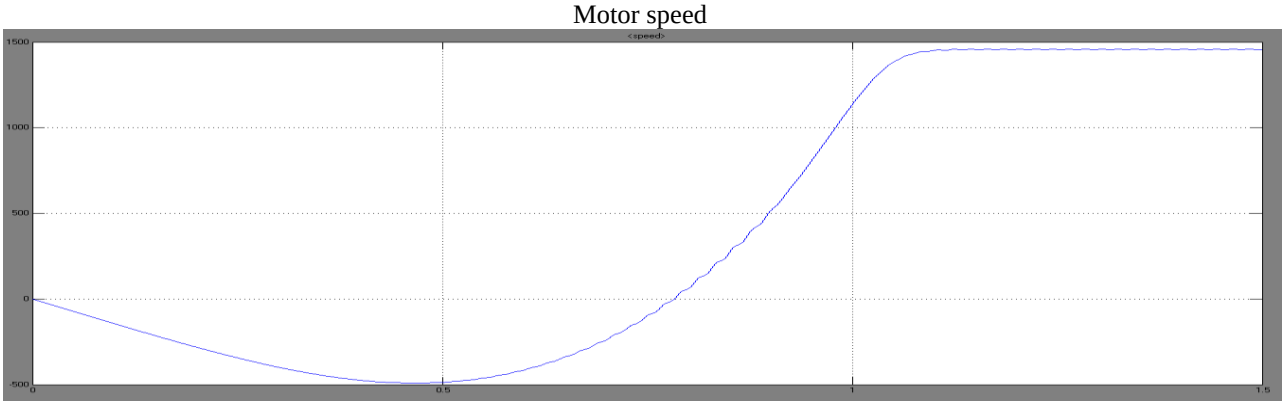


Fig. 6. Simulation results

V. CONCLUSION

In this project the SMC and its modulation method have been presented. The ZSMC is developed based on the circuit structure of an SMC and employs the Quasi network. This unique configuration enables the Quasi ZSMC to have a voltage boost feature and high reliability with less number of the power semiconductor switches than a traditional matrix converter. Furthermore, a current-compensation method based on an FLC has been presented to improve the output performance of the SMC under unbalanced input-voltage conditions. The simulation results confirm the boosting feature and the output performance of the Quasi network based SMC under unbalanced input voltage conditions using the proposed current-compensation method.

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BIOGRAPHY

Dr.Govindaraj Thangavel born in Tiruppur , India , in 1964. He received the B.E. degree from Coimbatore Institute of Technology, M.E. degree from PSG College of Technology and Ph.D. from Jadavpur University, Kolkatta, India in 1987, 1993 and 2010 respectively. His Biography is included in Who's Who in Science and Engineering 2011-2012 (11th Edition). Scientific Award of Excellence 2011 from American Biographical Institute (ABI). Outstanding Scientist of The 21st century by International Biographical centre of Cambridge, England 2011.

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