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Design And Implementation of 8T SRAM cell for Analysis of DC Noise Margin during Write Operation

Santhosh bg[1], Sowmya[2], Praveen J[3], Raghavengra Rao R[4]

M.Tech Student, Department of ECE, VLSI design and embedded systems, AIET, Mijar, Moodbidri, India[1]

Associate Professor, Department of ECE, AIET, Mijar, Moodbidri, Karnataka, India[2]

Sr. Associate Professor, Department of ECE, AIET, Mijar, Moodbidri, Karnataka, India[3,4]

Abstract: This paper focuses on the DC noise margin analysis and read/write failure analysis of the proposed 8T low power SRAM cell. In the proposed structure two voltage sources, one connected with the Bit line and the other connected with the Bit bar line for reducing the voltage swing during the switching activity. These two extra voltage sources will control the voltage swing on the output node and improve the stability. DC noise margin has been calculated by using loop gain technique and comparison made with that of conventional 6T SRAM justify the efficiency of the superiority of the proposed SRAM structure. Read and Write failure analyses are also done by using Monte-Carlo simulation. Simulation has been done in 65nm CMOS technology with 1 volt of power supply. Analog and schematic simulations have been done in 65nm environment with the help of Microwind3.1 by using BSimM4 model.

Keywords: CMOS; Dynamic power; DC noise margin; SRAM; Static Noise Margin; Voltage Swing

I. INTRODUCTION

Manufacturing of CMOS circuit variations can be classified as systematic or random. Systematic variations depend on factors such as layout structure and surrounding topological environment [1-2]. Random variations are caused by random uncertainties in the fabrication process such as microscopic fluctuations in the number and locations of dopant atoms in the channel region [3-4]. Random variations are harder to characterize and cause a significant mismatch in neighbouring devices and hence are largely responsible for the poor yield of the static random access memory (SRAM) arrays in scaled technologies [5-6].

Moreover, SRAM cells are traditionally designed to ensure that the contents of the cell do not get altered during read access while the cell should be able to quickly change its state during the write operation. These conflicting read and write requirements are satisfied by balancing the relative strengths of the devices in the design. Such careful design of an SRAM cell provides stable read and write operations, but it also makes the cell vulnerable to the failures caused by random variations in the device strengths. Due to increased sensitivity of SRAM designs to process variation, failure analysis of a memory cell has become an extremely important exercise. A modelling based approach cannot only be used to estimate cell failure probability in an efficient manner, but it can also guide cell optimization for yield enhancement

Analytical modelling of SRAM cell stability is not an old Concept. Earlier work in this field focused on characterizing SRAM robustness by modelling Static Noise Margin (SNM) of the cross-coupled inverters in a memory cell [7-8]. More recently, there have been efforts in characterizing cell stability during read and write operations. Most of these works rely on device equations to solve for parameters such as SNM, read disturbance and inverter trip-point. A number of recent literatures present the static and dynamic stability analyses of 6T, 7T, 8T, 9T SRAM cells for read and write operations [9-12]. All these papers used the butter fly diagrams to calculate the static noise margin (SNM) of the cross coupled inverters used in the SRAM cell for storing the data. Higher the SNM value, higher will be the stability of the SRAM cell.

The paper is organized as follows: Section II discusses ab -out the Conventional 6T SRAM cell, Section III describes circuit design and working principle of the proposed novel 8-T SRAM cell. Section IV describes the detailed analysis of DC noise margin of the proposed SRAM cell. Section V shows the write stability failure analysis. In section VI the read stability failure analysis has been discussed, and finally section VII concludes the paper

II. LITERATURE REVIEW

A. Conventional 6T SRAM cell

Figure 1 shows the circuit diagram of a conventional SRAM cell. Word line (WL) is used for enabling the Access transistors T2 and T5 for write operation [13]. BL and *BL* lines are used to store the data and its compliment. For write operation one bit line is high and the other bit line is on low condition. For writing "0", BL is Low and *BL* is high. When the word line is asserted high, transistors T2 and T3 are ON and any charge stored in the BL goes through T2-T3 path to ground. Due to zero value at Q, the T4 transistor is ON and T6 is OFF. So the charge is stored at Q bar line. Similarly in the write "1" operation, BL is high due to this T6 is ON and the charge stored on the Q is

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discharged through the T5-T6 path and due to this low value on the Q, T1 is ON and T3 is OFF, so the charge is stored on the Q.

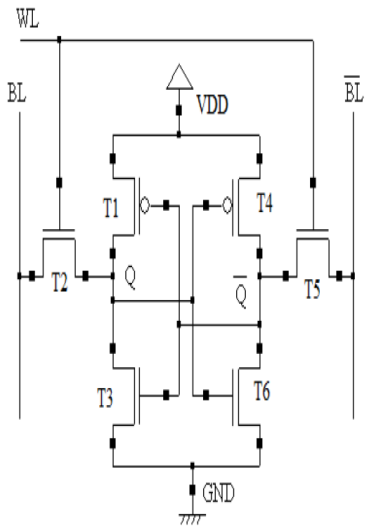

Figure 1. Conventional 6T SRAM cell.

Before the read operation begins, the bit line BL and the bitbar line *BL* are pre-charged to as high as Vdd. When the WL is selected, the access transistors T2 and T5 are turned ON. This causes a current to flow from Vdd through the pull-up transistor T1 of the node storing "1".On the other side, current will flow from the pre-charged bitbar line to ground, thus discharging *BL* line. Thus, a differential voltage develops between *BL* and *BL* lines. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output. Conventional 6T SRAM cell works on the full voltage swing. This means that if the operating frequency of the SRAM cell is increased then the dynamic power dissipation will also be increased. Hence, for high speed CMOS operation the conventional SRAM cell is not a good choice. Also conventional 6T SRAM cell has been found to be unstable beyond below 130nm technology and results in low read static noise margin (SNM).

III. PROPOSED SRAM CELL

In the proposed design two voltage sources VS1 and VS2 are used and are connected to the outputs of the *BL* and *BL* lines, respectively. Two NMOS transistors VT1 and VT2 are connected, respectively, with inputs of bit and bit bar lines directly to switch ON and switch OFF the power source supply during write "0" and write "1" operations, respectively. The proposed design has been illustrated in Figure 1. These power supply sources reduce the voltage swing at the 'out' node when write operation is being performed.

A. Write '0' operation

During the write '0' operation, *BL* line is Low and *BL* line goes high. So the transistor VT2 is ON and the transistor VT1 goes to OFF condition. Thus the voltage source VS2 forces to decrease the voltage swing at output of the *BL* line.

B. Write '1' operation

Similarly when we perform the write '1' operation, the transistor VT1 is ON and the transistor VT2 goes to OFF condition, so the voltage source VS1 decreases the voltage swing at the BL output.

Due to the decrease in voltage swing, dynamic power dissipation is almost constant even if we increase the frequency of the SRAM cell.

The dynamic power may be expressed as

$$P_{dynamic} = \alpha C V_{dd} V_{Swing} f$$

where C = Load capacitance's = Activity factor; f =Clock frequency; V = Voltage swing at output node.

So as the frequency increases the dynamic power dissipation also increases because the dynamic power depends upon the operating frequency [14].

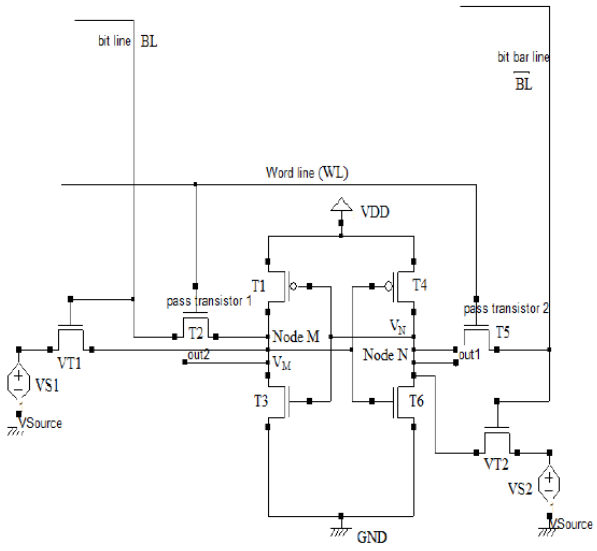

Figure 2. The Proposed 8T SRAM Cell.

In the proposed SRAM model voltage sources VS1 and VS2 decrease the voltage swing during switching activity. As the frequency increases the switching activity will also be increased but voltage sources decrease its voltage swing simultaneously at the output. So at higher frequency the dynamic power dissipation is almost constant. These two voltage sources also provide extra voltage during the read/write operation on the *BL* line, *BL* line and *WL* line. This extra voltage will provide the better noise margin on bit lines and word line during read/write operations.

For controlling the noise margin during write operation, the sizes of the transistors are a major concern. The rule of thumb is that the width ratio of the transistors T1 and T2 is nearly equal to 1.5 and the width ratio for T2 and T3 is also equal to 1.5. Similarly it is applicable for transistors T4, T5 and T6, respectively.

$$\frac{W_1}{W_2} \approx \frac{W_2}{W_3} \approx 1.5 \text{ and } \frac{W_4}{W_5} \approx \frac{W_5}{W_6} \approx 1.5$$

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This size configuration provides the proper driving voltage to transistors for ON and OFF conditions.

IV. DC NOISE MARGIN ANALYSIS

The DC noise margin of an SRAM cell is described as the minimum amount of DC noise required to change the state of the cell. Basically it is calculated by measuring the side of the longest square that can be present between mirrored DC characteristics of the cross-coupled inverters in a memory cell.

Figure 3 shows the static noise margin (SNM) curve for the proposed SRAM cell.

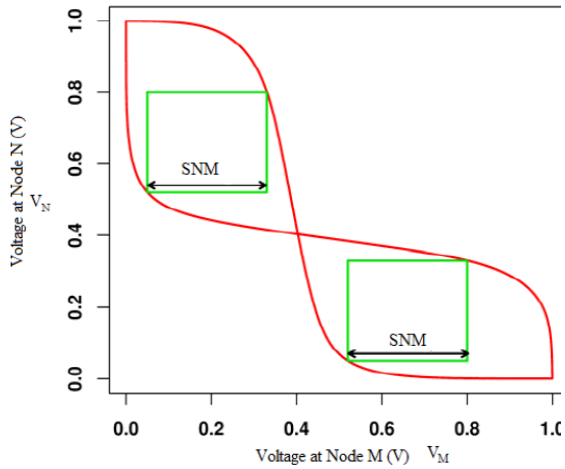

Figure 3:Static Noise Margin curve for the Proposed SRAM cell.

In this section, a loop gain concept has been used for measuring the DC noise margin. Firstly consider the case when an SRAM cell stores a value (VM = 0 and VN = 1) and a DC noise disturbance at node M causes its potential VM to rise above zero. The main objective is to find the minimum DC noise disturbance at node M that causes the cell to lose its present state. The DC transfer characteristics of inverters used in proposed SRAM cell can be modelled by functions *f* and *g*, respectively. For a symmetric cell, the two functions should be identical, but they will differ due to random mismatches in the device characteristics.

Due to the non-linear nature of the transfer-characteristics *f* and *g*, the gains of the two inverter stages T1-T3 and T4-T6 depend on their input voltages. Hence a disturbance at node M causes a change in the gain of the inverters. A noise offset at node M also changes the potential at node N and hence impacts the gain of the feedback stage.

Figure 4 shows the value of VM that causes the loop gain to become unity. This value, labelled as VM in the Figure 4,represents the minimum DC potential required to flip the contents of a cell. In other words, VM (flip) is the maximum potential that can be tolerated by node M without altering its state from zero to one. Table I shows that the proposed SRAM cell has higher DC noise margin value than the conventional SRAM cell which shows the higher stability of the proposed SRAM cell.

V. READ STABILITY FAILURE

The chances of failure of SRAM cell is more during read operation than during write operation. For performing the read operation firstly the bit lines are pre-charged to Vdd, then the contents of the cell through the access transistors are read. When the access transistors are turned on, one of the precharged bit lines discharges through the access device and the inverter pull-down transistor. In Figure 2, during a read access, the bit line BL will discharge through the access transistor T2 and the pull-down transistor T3 to read a zero at node M. This method of reading cell contents exposes the internal storage node M to the disturbance caused by the resistive voltage division between the access transistor and the pull down transistors. This disturbance is minimized by making the pull-down transistor much stronger than the access transistor

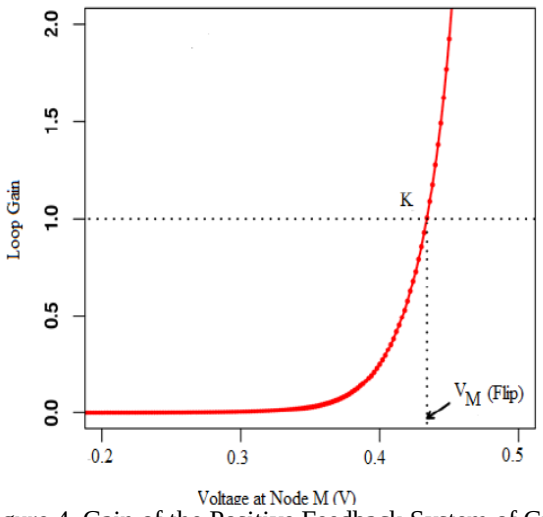

Figure 4. Gain of the Positive Feedback System of Cross-coupled Inverter at Node M.

However, random variations in the threshold voltages and therefore the strengths of various transistors in an SRAM cell can cause the read operation to flip the contents of the cell. These failures are defined as read stability failures. Read stability failures can be analyzed in a similar manner. The DC noise analysis is valid because the read access time is usually larger than the time required flipping the state of the cross-coupled inverters. When the word line (WL) is turned ON, a noise voltage is immediately developed at the internal node of the cell. The WL stays high for duration long enough for the bit line to discharge by a specific value. During this period, if the DC noise voltage at the internal node is large enough to flip the contents of the cell, the cell loses its state resulting in the read stability failure. The read stability of a cell can be analyzed by computing the loop gain of the system in read mode. The forward and the feedback characteristics are computed by including access transistors along with the inverters as shown in Figure 5.

The read noise margin (RNM) can then be expressed as

$$RNM = V_M - g[f(V_M)]$$

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RNM is a useful metric in analyzing read stability failures. The RNM value for the proposed SRAM cell is 0.467 volt. A positive value of RNM represents a stable read operation while a zero or negative value of RNM signifies that the read operation will cause the cell to lose its state resulting in the read stability failure. We characterize the impact of random variations on RNM through SPICE-based Monte-Carlo simulation in an industrial 65 nm
nm technology. The simulation models the threshold voltage of each transistor in the cell as an independent

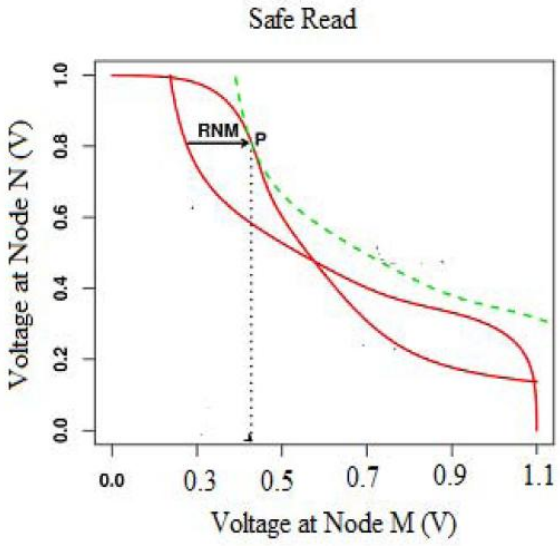

Figure 5. DC Transfer Characteristics curve for Read Operation.

random variable. The threshold tolerances for different transistors in the cell are chosen from the technology specifications and include the dependence of sigma-VT on device width.

VII. CONCLUSIONS

Stability is a major issue in high speed CMOS VLSI D design. In this paper a low dynamic power consuming and highly stable SRAM cell has been proposed. This proposed SRAM cell has two voltage sources which are used for reducing the swing voltage during switching activity. The reduction in voltage swing results introduction of dynamic power dissipation as well as improves the stability during write/read operation. The proposed SRAM cell is more stable in comparison to conventional 6-T SRAM cell. DC noise margin of the proposed SRAM has been calculated by using loop gain technique and the results are compared to those of conventional 6T SRAM cell. The value of DC noise margin is 0.439 volt which shows the higher stability for the proposed SRAM cell. Monte-Carlo simulations are also carried out for read and write failure analyses. This simulation shows that the proposed SRAM cell has lesser probability of read/write failure and worked properly during both read and write operations. Although numbers of transistors and area are increased in comparison to those of conventional SRAM cell but low power dissipation and higher stability can easily dominate over this drawback. This proposed SRAM cell can be used to provide low power solution in high speed devices like laptops, mobile phones, programmable logic devices etc.

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