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Efficient Power Conservation using adiabatic subtracter

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Abstract: Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic. The adiabatic logic uses AC power supply instead of constant DC supply.This is one of the main reasons in the reduction of power dissipation. This paper describes implementation full subtractor. The simulation results of CMOS design are compared with different adiabatic logic styles such as efficient charge recovery logic (ECRL) and positive feedback adiabatic logic (PFAL).The simulation results indicate that the proposed technique is advantageous in many of the low power digital applications. The design is implemented using Tanner tool.

Keywords: Low Power, Energy Recovery, Adiabatic logic,ECRL.

I. INTRODUCTION

Over the past few decades, low power design solution has steadily geared up the list of researcher's design concerns for low power and low noise digital circuits to introduce new methods to the design of low power VLSI circuits. Hence the obvious need is to develop circuits which dissipate less amount of power and perform more functionality. This need is further apprehended by the space industry and hand held devices where devices are needed to operate at limiting power availability through batteries for a very large amount of time.

A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Just losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit. Many adiabatic logic families have been proposed.

We are focusing on a novel energy efficient technique called adiabatic logic [1] which is based on energy recovery principle. In this technique instead of discharging the consumed energy is recycled back to the power supply thereby reducing overall power consumption. In this performance of subtracter is evaluated in different adiabatic logic styles and their results were compared with the conventional CMOS design.

In CMOS design it is evident that during the charging process, the output load capacitor is charged to Q = $C_L V_{dd}^2$ and the energy stored at the output is ½$C_L V_{dd}^2$. During the discharging phase, the amount ofenergy dissipated is also ½$C_L V_{dd}^2$. So the total amount of energy dissipated during the charging and discharging phases is

$$E_{dissipated} = C_L V_{dd}^2 \quad \ldots\ldots\ldots \quad (1)$$

The power consumption of the CMOS circuit is based on the following equation

$$P = C_L V_{dd}^2 f \quad \ldots\ldots\ldots\ldots \quad (2)$$

From the equation it is evident that the power dissipation of CMOS can be reduced by minimizing the supply voltage, node capacitance and switching activity to some extent. But reducing the values of these parameters may suffer from some disadvantages. Reducing the load capacitance is strongly limited by the technology. Reducing the supply voltage [2] may degrade the performance of the device. Reducing the supply voltage may also suffer from leakage problems. In order to overcome these problems an efficient low power technique called adiabatic logic has been implemented.

II. CMOS FULL SUBTRACTOR

Arithmetic circuits are the most important elements in the design of many VLSI digital circuits. We must design chips in such a way that it must consume less power and dissipation less power with efficient output. Full subtractor is one of the arithmetic circuits which is widely used in internal chip design of many digital circuits. It has three inputs and two outputs which are difference and borrow.

TABLE 1
Truth Table for full subtractor

A	B	C	DIFF	BORR
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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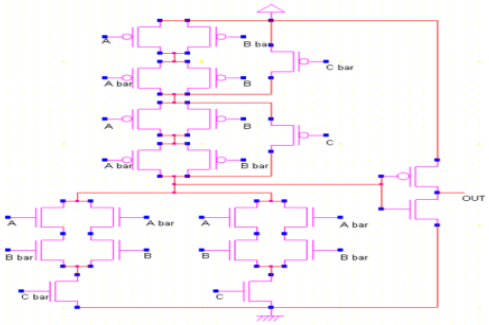

Fig.1Circuit for CMOS Difference

Fig. 2 Waveform for CMOS Difference

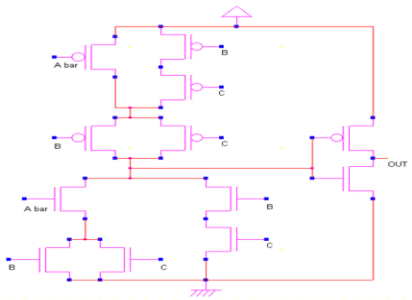

Fig.3. Circuit for CMOS Borrow

Fig4. Waveform for CMOS Borrow

III.EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Efficient charge recovery logic consists of two cross couple PMOS transistors in the pull up section where as the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to Cascode Voltage Switch Logic (CVSL) with differential signalling. The logic function in the functional block can be realized with only NMOS transistor in pull down section.[1]

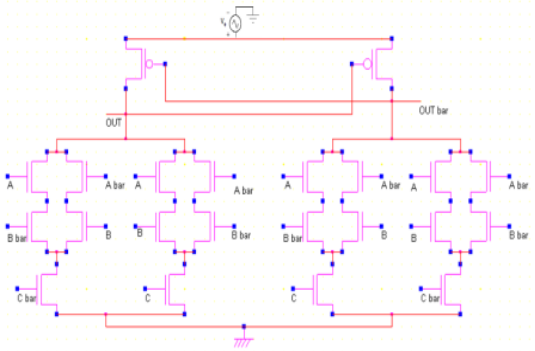

Fig 5. Circuit for ECRL Difference

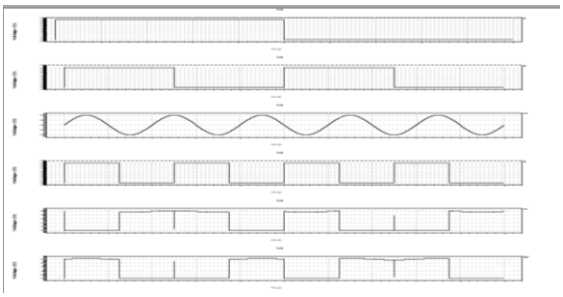

Fig6 Waveform for ECRL Difference

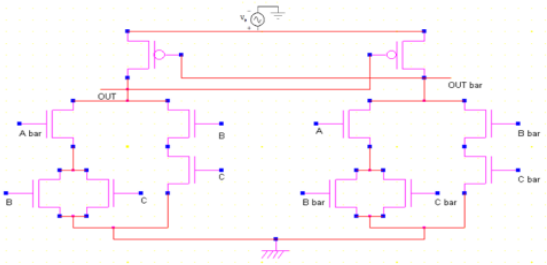

Fig7. Circuit ECRL Borrow

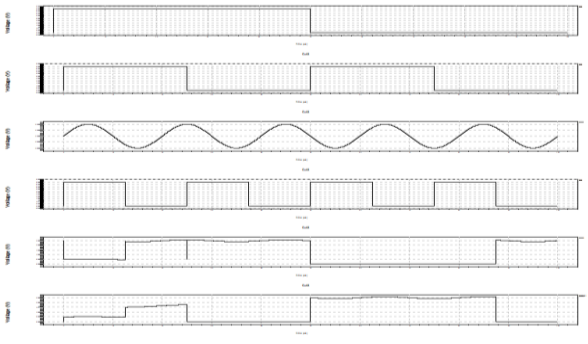

Fig. 8 Waveform for ECRL Borrow

\Positive Feedback Adiabatic Logic (PFAL)

PFAL is new adiabatic technique which utilizes positive feedback. This logic structure consists of cross-coupled inverters, with NMOS devices are connected between the outputs and the power-clock. In PFAL, sinusoidal power supply is used, known as power clock which is divided into four phases.3 In evaluate interval, the outputs are evaluated from stable input signal. During hold interval, output are kept stable, next is the recover interval, which recover the energy and the last is wait interval, inserted for

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the symmetry. PFAL is a dual-rail circuit which accept complementary inputs with respect to each other and provide outputs complemented with each other with partial energy recovery [2].

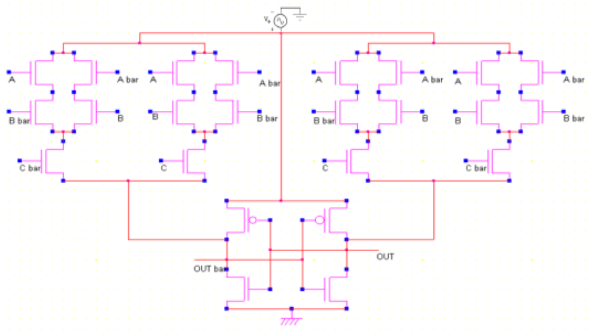

Fig 9.Circuit of PFAL Difference

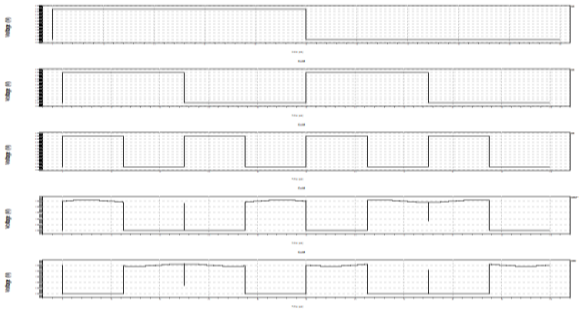

Fig. 10 Waveform for PFAL Difference

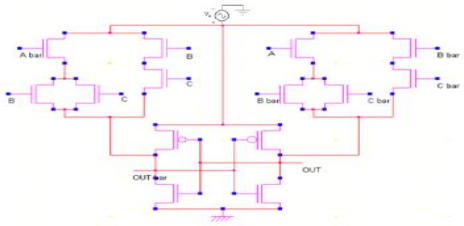

Fig 11.Circuit of PFAL Borrow

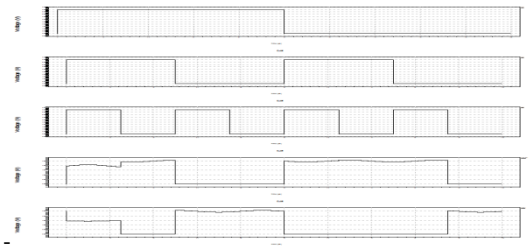

Fig. 12 Waveform for PFAL Borrow

vPOWER ANALYSIS

TABLE 2
Comparison of Power Dissipation

	DIFFERENCE	BORROW
CMOS	8.37 mW	5.56mW
ECRL	25uW	142.5uW
PFAL	122.5uW	106.25uW

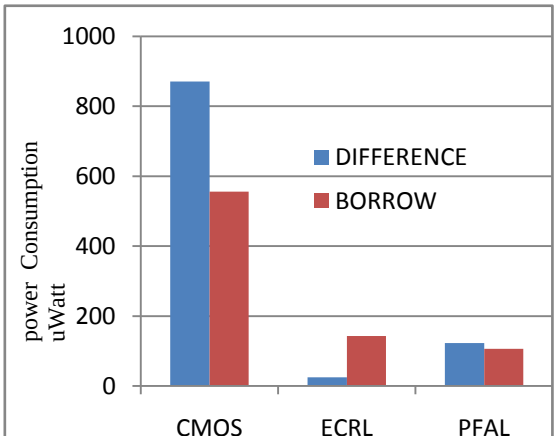

Fig.13. Comparative analysis of power consumption

CONCLUSION

Adiabatic circuits consume very less energy consumption as compared to conventional CMOS circuits. Power reduction is possible with proper choice of Adiabatic family and substrate bias voltage selection. This low power design methodology can be used in designing implantable biomedical devices or in any battery operated circuit which processes low frequency signals.

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