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High Speed IP Based Architecture for Telecommand System on chip (SoC)

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Abstract: An IP (intellectual property) core is a block of logic or data that is used for making a field programmable gate array (FPGA) or application-specific integrated circuit (ASIC) for a product. Design reuse IP cores are part of the growing electronic design automation (EDA) industry which allows the repeated use of previously designed components. Using many IP cores a system itself can be designed, System on Chip (SoC) offers this requirement. In the current telecommand communication method, excess number of physical devices is present, which cause a major communication delay. Combining many of the predesigned internal blocks in to a single chip can solve this problem. The paper is concerned with the design of telecommand and telemetry system and its peripheral devices like combined memory and error detection and correction (EDAC) unit.

Keywords: EDAC, Telecommand, SoC.

I. INTRODUCTION

The semiconductor industry has continued to make impressive improvements in the Very Large-Scale Integrated (VLSI) circuits. In order to keep pace with the levels of integration available, design engineers have developed new methodologies and techniques to manage the increased complexity occurs in these large chips. One such emerging methodology is system-on-chip (SoC) design, wherein predesigned and pre-verified blocks often called intellectual property (IP) blocks, IP cores, or virtual components obtained from internal sources, or third parties, and combined on a single chip. These reusable IP cores may include embedded processors, memory blocks, interface blocks, analog blocks, and components that handle application specific processing functions. Corresponding software components are also provided in a reusable form and may include real-time operating systems and kernels, library functions, and device drivers.

A System on a Chip or System On Chip (SoC or SOC) is an Integrated Circuit (IC) which integrates all the components of a computer or any other electronic system into a single chip. It is a group of all components and it's subcomponents of a system on to a single chip. SoC design allows high performance, miniaturization, good process technology, cost sensitivities and an efficient battery life time. This innovation in design had been used by many designers .Advantages includes the high performance and low power consumption, cost, and size.

A telecommand is a command sent to control remote system or systems i.e. not directly connected (e.g. via wires) to the place from which the telecommand is sent. The telecommand word is derived from tele = remote (Greek), and command = to entrust/order (Latin). Systems that need remote measurement and reporting of information of interest to the system designer or operator, require the counterpart of telecommand, telemetry. For a telecommand (TC) to be effective, it must be compiled into a pre-arranged format (which may follow a standard structure), modulated onto a carrier wave which is then transmitted with adequate power to the remote system. The remote system will then demodulates the digital signal from the carrier, decode the telecommand, and execute it. Transmission of the carrier wave can be by ultrasound, infra-red or other electromagnetic. For effective control of the various satellite sub-systems under all conditions, a highly efficient and responsive telecommand (TC) system is absolutely essential. Some of the important operations performed by the telecommand system include energizing various subsystem, tape recorder operations, spin-up of satellite etc. Since remote control through telecommand system is the mainstay for these operations to be reliably performed in the satellite in orbit, the system has to work with a high degree of reliability design wise. Inclusion of many physical devices in the whole communication system always makes communication delays. Combining certain blocks of system can reduce such delays.

II. LITERATURE SURVEY

The work titled "designing of telecommand system using SoC for space craft control application"[5] , describes the importance of checking the integration between components in the whole system and advantage of using pre-defined and pre-verified IP units in space communication like telecommand system. In the paper "FPGA implementation of SoC architecture for space craft application" introduces the UART (Universal Asynchronous Receiver and Transmitter) to transmit data in to ground station and implementation of entire system in to FPGA, which is a future work of [5].

But the architecture using VIRTEX 5 FPGA device makes a tradeoff between frequency and time delay with 48% increase in operating frequency and having a minimum time delay of about 5%.

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The work titled "system on chip: reuse and integration" deals with the introduction of IP based blocks which are reusable in nature. It also describes the possibility of integration of many such units in to a single chip i.e. SoC designs. [7]

III. DESIGN METHODOLOGY

This paper can be implemented as the telecommand System-on-a-Chip (SoC) in the On-Board System (OBS). For that each unit in the entire system treated as IP cores. To build the system on-a-chip, hardware description language VHDL is used. The overall telecommand system is the integration of SRAM, PROCESSOR and EDAC Unit. To overcome the shortfall of the present design where the major drawback has been the increased delay and decrease in frequency for transmission of data packets, the new architecture is designed as shown in Figure 1. [20]

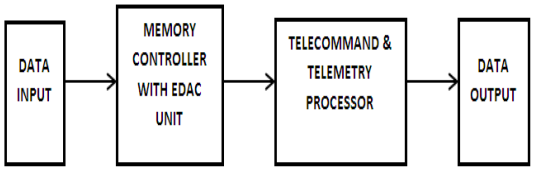

Figure 1: Block diagram of SoC design

A. Design of SRAM

Static random-access memory (SRAM) is a type of semiconductor memory. For storing bits in the memory it uses the bistable latching circuitry. SRAM is a volatile memory, means data will loss when the memory is not powered. But still it has significance in terms of speed of access. The other type of memory DRAM (Dynamic RAM) can delete the data as well as refresh while running the program.

The basic architecture of a static RAM contains rectangular arrays of memory cells with support circuitry. Depending on the data to be stored, cell numbers vary. The support circuitry is used to decode addresses, and to implement the required read and write operations .The block diagram of 2k x 32 bit SRAM is shown in Figure 2.

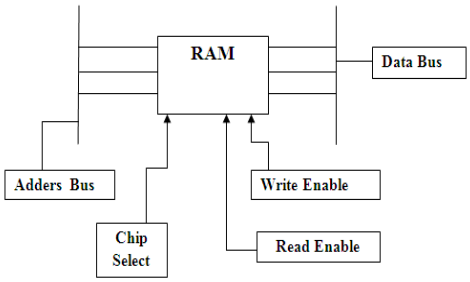

Figure 2: Block diagram of 2K x32 bit SRAM

SRAM memory arrays are arranged in rows and columns and each section is called a memory cell. The rows are called word lines and the columns are called bit lines. A memory cell is said to be a unique location or address defined by the intersection of a row and column. This intersection is linked to a specific data input/output pin. Number of arrays on a memory chip is determined by certain parameters. They include the speed at which the memory must operate, total size of the memory, the number of data inputs and outputs on the chip and layout and testing requirements. Memory arrays are considered as the vital building block for designing as well as implementing any digital systems. Memory size is large for any of the digital system. Physical area takes for the SRAM can calculated as follows. For an Nxn SRAM array where 'N' indicates the number of bytes and 'n' indicates the byte size. The size of an SRAM with m address lines and n data lines is 2/\m words, or 2^ m x n bits

B. Design of EDAC unit

In information theory and coding theory with applications in computer science and telecommunication, error detection and correction or error control are techniques that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection means to decide whether the received data is correct or not without having a copy of the original message.Error detection uses the concept of redundancy, which means adding extra bits for detecting errors at the destination.[1]

An error-correcting code (ECC) is a system of adding redundant data, or parity data, to a message, such that it can be recovered by a receiver even when a number of errors (up to the capability of the code being used) were introduced, either during the process of transmission, or on storage. The modified Hamming Code is widely used for Single-Error Correctable and Double-Error Detectable (SEC-DED) codes. The code format is as shown in Figure 3.

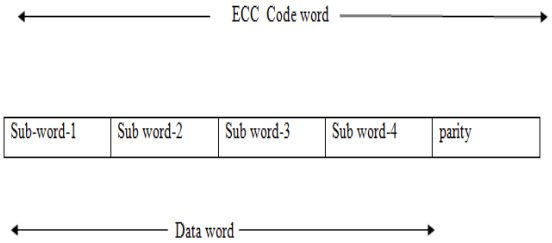

Figure 3: ECC code word format

C. Integration of SRAM with EDAC unit

A low Earth orbit (LEO) is an orbit around Earth with an altitude between 160 kilometres (99 mi), (orbital period of about 88 minutes), and 2,000 kilometres (1,200 mi) (about 127 minutes). All manned space stations to date, as well as the majority of satellites, have been in LEO. The data stored in LEO are digital in nature. These digital data always have undergone some kind of disturbances. SEUs (single event upset) is the main among them. It is caused by radiations like UV, IR and gamma radiations. This adversely effects memory chips. Error detection and correction techniques are helpful to handle this problem.

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For the secure transaction of data between the CPU of the on board computer and its local RAM, the program memory has generally been designed by applying the Hamming code.

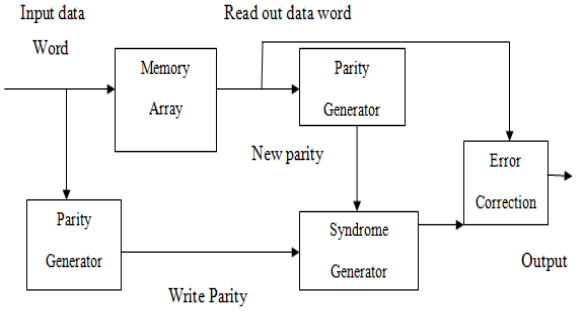


Figure 4: Integration of SRAM with EDAC unit

In the error control the designation (n, k) denotes a block of code that takes a k-bit data word and maps it to an n-bit code word. The importance of reducing the size as well as integration of units is here. There is a chance of occurring two bit error in a single byte. Before the second error comes the first error should clear by the computer. In the Fig.4 the Parity Generator generates the parity from the input data word. The entire code word, which includes the data word and parity word, is written into the memory when it performs the WRITE operation. In a READ operation, the data word to be read is used to generate the parity again. The Syndrome Generator compares the newly generated parity with the read-out parity to produce the syndrome that contains the information for error bits. The Error Corrector corrects the error in the read-out data word if necessary, based on the Syndrome.

D. Telecommand Processor

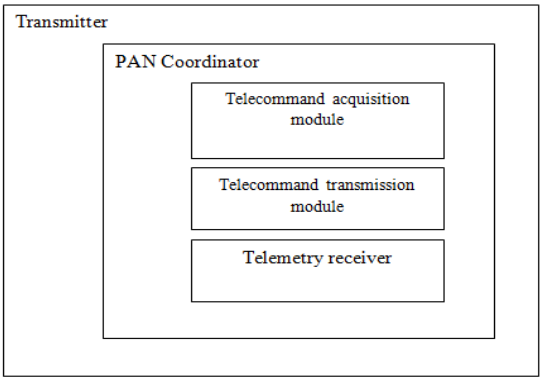


Figure 5: Block diagram of telecommand transmitter

In spacecraft application requirement, the star topology is selected, it is simple to implement and it has less complexity and it satisfies all the requirements of TC-TM systems. The PAN coordinator and FFD's are devices and they are configured as star topology.

The PAN coordinator is interfaced with both TC and TM systems as shown in fig 5. The FFD's are interfaced with other subsystems of the satellite as shown in fig 6. In PAN coordinator, received command from the EDAC unit and transfer to the Full Function Devices (FFD's) in subsystems and intended FFD receives command. It is decoded and converted as pulse or level or data command and it is executed in the subsystem end. Each FFD can execute any number of commands as required by the subsystems. In this fashion commands are distributed to subsystems through FFD's in wireless mode. The FFD's receives different heath parameters and payload data from respective subsystems and transmits to PAN coordinator.

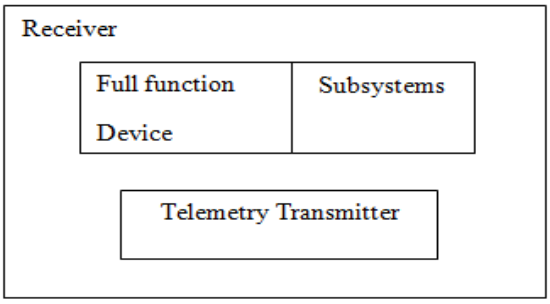
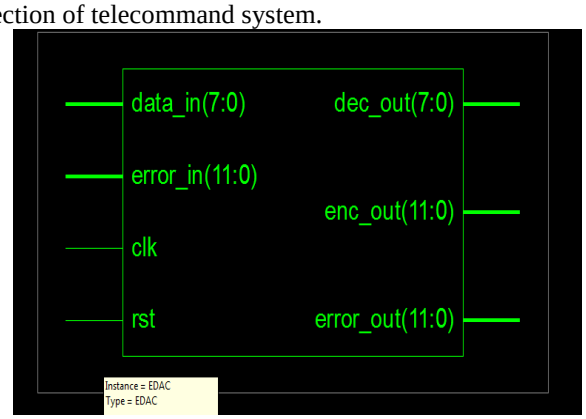


Figure 6: Block diagram of Telecommand receiver

IV. RESULTS AND DISCUSSIONS

Results show the RTL schematic of EDAC unit, the simulation result of the RAM memory and transmitter section of telecommand system.



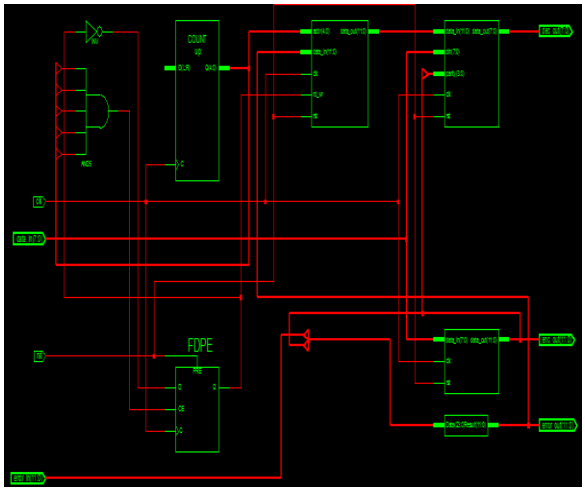


Figure 7: RTL Schematic of EDAC unit.

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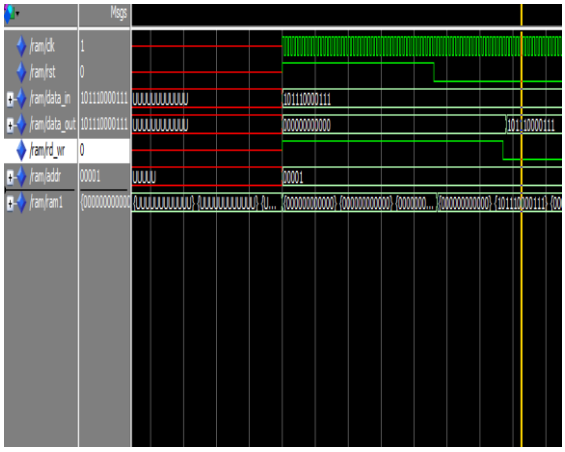

Figure 8: Simulation result of RAM memory.

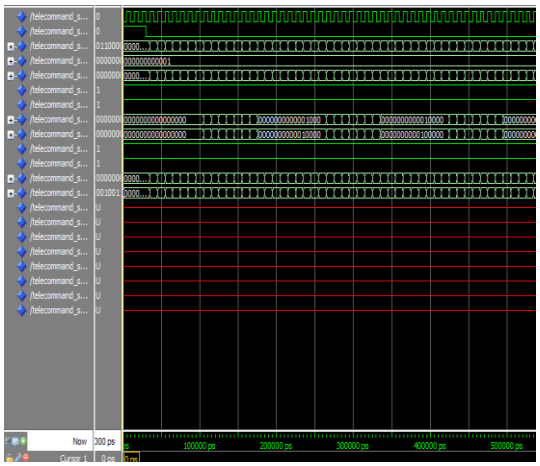

Figure 9: Simulation result of telecommand transmitter.

Future works include its ASIC design and its implementation.

V. CONCLUSION

Consumer demands for high performance and rich functionality have driven the semiconductor manufacturing industry to the integration of multiple complex components onto a single chip. As the complexity of the remotely located physical devices increases, the requirement for a greater telecommanding capability and efficiency arises, but present IP Core Based Architecture of telecommand System-on-a-Chip (SoC) has increased delay in transmission of data packets. By decreasing the delay system get better throughput and increase its features. The new architecture is designed to analyze the scope for a performance enhancement with respect to the present system.

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