ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3, Special Issue 1, April 2015

Design and Analysis of an Efficient Wallace Tree Multiplier using Current Comparison Domino

Akshatha K[1], Mrs. Savitha M[2]

M.TECH. Student VLSI & ES Department KVG College of Engineering Sullia, India[1]

Associate Professor E&C Department KVG College of Engineering Sullia, India[2]

Abstract: In this paper, a new domino circuit is proposed with low leakage current and high noise immunity which decreases the parasitic capacitance on the dynamic node. This yields a smaller keeper transistors for wide fan-in gates to implement fast and robust circuits. The technique utilized is based on comparison of mirrored current of the pull-up network with its worst case leakage current. Thus, the power consumption and delay can be reduced. A 6*6 Wallace tree multiplier is designed based on CCD (Current Comparison Domino) which uses low leakage high speed full adders. These full adders uses current comparison based domino logic to achieve low leakage and high speed. The proposed design is simulated using LT SPICE schematic editor tool.

Keywords: Current Comparison Domino (CCD), Pull Up Network(PUN),Pull Down Network (PDN) ,Wallace Tree Multiplier.

I. INTRODUCTION

The main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (Vth) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the subthreshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs. However, in wide fan-in dynamic gates, robustness and performance significantly degrade with increasing leakage current. Another drawback is due to the existance of inter device capacitance of NMOS array will lead to reduction of charge across the load. As a result, it is difficult to obtain satisfactory robustness–performance tradeoffs[1].

In domino logic scaling the supply voltage and capacitance of dynamic (pre-charge) node reduces the amount of charge stored at the dynamic node. Due to these concurrent factors, the noise immunity of domino gate substantially decreases with technology scaling. Wide fan-in domino logic has many applications in digital signal processors and high performance critical units of microprocessors. The Multipliers play a major role in arithmetic operations in the digital signal processing application. Currently the need for low power multiplier has been increased due to the increasing demand for portable and mobile systems.

In this paper an efficient Wallace tree multiplier is designed using CCD full adders. The replacement of normal full adders by domino logic full adders in the multiplier increases the performance and reduces the leakage power consumption and also the delay compared to the other domino logic styles [2].

II. CONVENTIONAL DOMINO LOGIC DESIGNS

Some of the conventional domino circuits which are used later for performance comparison are shown below.

A. Conditional Keeper Domino (CKD)

The conditional keeper domino logic (CKD) is another domino circuit shown in Fig. 1. The circuit consists of a small and a large transistor. The smaller keeper transistor (K1) is ON if the dynamic node is high to avoid voltage drop on the dynamic node. After a certain delay during the evaluation phase, the output of the NAND gate become slow to turn on K2, if the dynamic node is still high. The state of the dynamic node is maintained by K1 at the beginning of the evaluation phase, and by K2 at the rest of the evaluation phase. However, CKD circuit has some drawbacks such as limitations on decreasing delays of the inverters and the NAND gate to improve noise immunity. Upsizing of delay inverters can improve noise immunity, but will instead result in significant power dissipation.

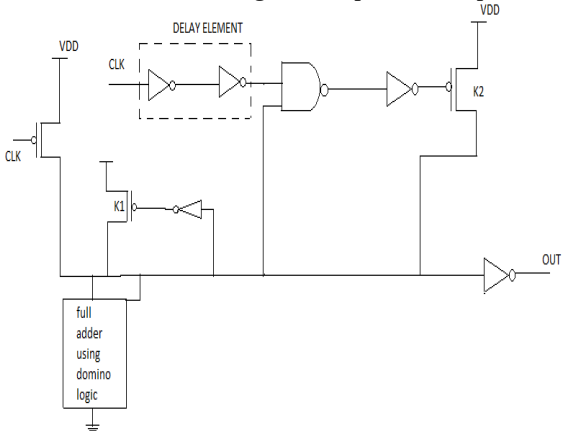

Fig 1. Conditional Keeper Domino Logic (CKD)

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2.2 High Speed Domino Logic(HSD)

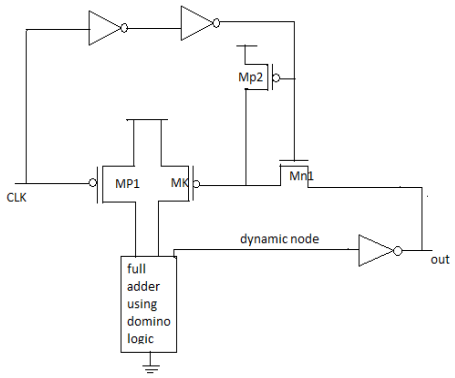

Fig 2. High Speed Domino Logic(HSD)

High speed domino logic (HSdomino) shown in Fig 2. HS has a different keeper control scheme. In this circuit, when the clock is switched to high, the NMOS transistor Mn1 is still off and the PMOS transistor MP2 is still on. Thus, MP2 turns off the keeper transistor MK. MP2 is turned off after the delays of the inverters. If the dynamic node remains high during the evaluation phase, the NMOS transistor is turned on and turns on the keeper transistor. Since the dynamic node at the beginning of the evaluation phase is a float, in the absence of the keeper transistor any noise at the inputs could cause the evaluation node to be discharged. Also gate of MK can be at VDD-VtMn1, where VtMn1 is the threshold voltage of the NMOS transistor Mn1. This would result in a DC current flow through the PMOS keeper transistor and the NMOS network[4].

III. PROPOSED CCD

Since in wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems would be solved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. This idea is is illustrated in Fig3. Here transistor *MK* is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage.

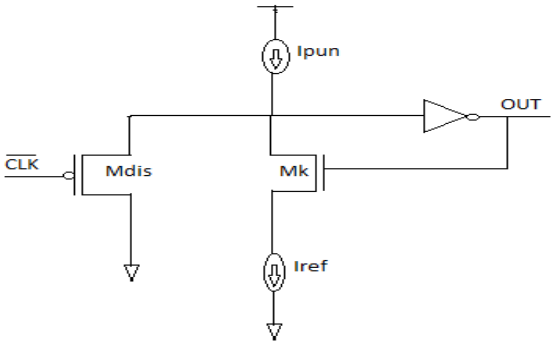

Fig3: Concept of proposed circuit (CCD)

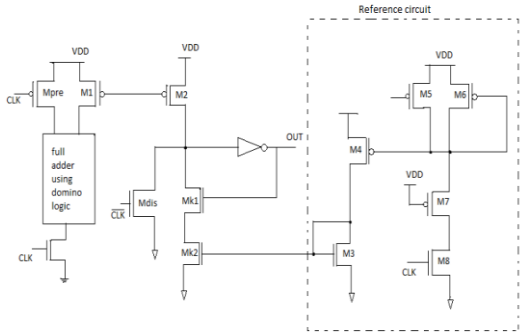

Fig 4. Implementation of full adder using current comparison based domino logic

An important issue in the generation of the reference voltage, which is the correct variation of the reference current according to the process variations to maintain the robustness of the proposed circuit.

The proposed circuit is operated in two modes, predischarge mode and evaluation mode.

Predischarged mode,

The input signals and clock voltage are in high and low levels respectively, [CLK = "0", CLK = "1" in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor M_D is and raised to the high level by transistor M_{pre}, respectively. Hence, transistors M_{pre}, M_{Dis}, M_{k1}, and M_{k2} are on and transistors M_1, M_2, and M_{Eval} are off. Also, the output voltage is raised to the high level by the output inverter.

Evaluation mode

Clock voltage is in the high level [CLK = "1", CLK = "0" and input signals can be in the low level. Hence, transistors M_{pre} and M_D is are off, transistor M_1, M_2, M_{k2}, and M_{Eval} are on, and transistor M_{k1} can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor M_1 due to the leakage current. Although this leakage current is mirrored by transistor M_2, the keeper transistors of the second stage (M_{k1} and M_{k2}) compensate this mirrored leakage current. It is clear that upsizing the transistor M_1 and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor M_1. This voltage is also equal to drain-source voltage of M_1 and depends on size of M_1 and its current. Increasing the pull-up current increases the

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mirrored current in transistor M_2, thus voltage of the dynamic node Dyn is charged to V_{DD}, yielding discharging the voltage of the output node and turning off the main keeper transistor M_{k1}. By this technique the contention current between the keeper transistor and the mirror transistor is mitigated. Here dynamic power dissipation is reduced in the evaluation mode[3].

IV. WALLACE MULTIPLIER

A 6*6 Wallace tree multiplier is designed using current comparison based domino logic full adders is as shown in fig 5. 6*6 Wallace multiplier has 27 full adders, where all these full adders are replaced by current comparison based domino logic full adders. By these adders dynamic power dissipation in the multiplier is reduced such that half of the total leakage power of Wallace tree multiplier is reduced.

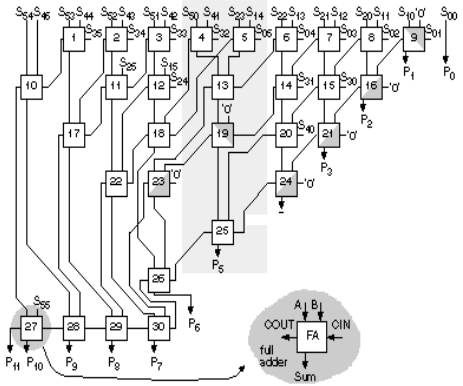

Fig 5. 6*6 Wallace Tree Multiplier

V. RESULTS AND ANALYSIS

The design is simulated using LT SPICE schematic editor tool. The simulation waveform obtained for various domino circuit is shown below.

Fig .6. shows the schematic diagram of proposed CC domino and Fig.7 shows the simulation result which is obtained by simulating this design in LT SPICE schematic editor tool and is same as expected. Fig .8. shows the schematic diagram of proposed Wallace tree multiplier. Fig 9.shows the expected graph of the proposed and conventional results in terms of delay and power.

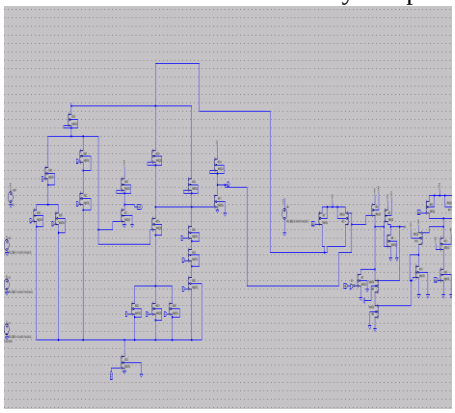

Fig 6. schematic diagram of proposed CC domino

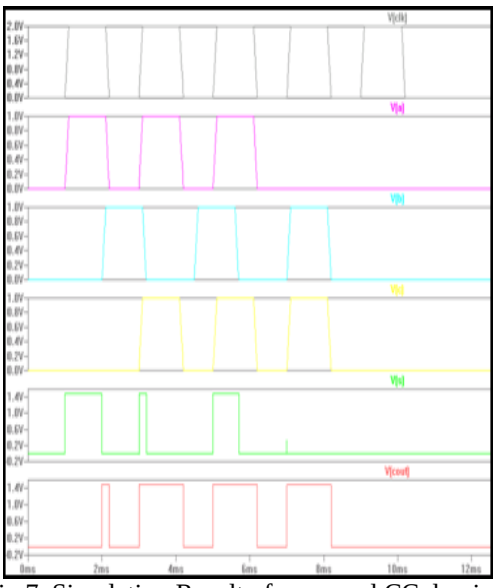

Fig 7. Simulation Result of proposed CC domino

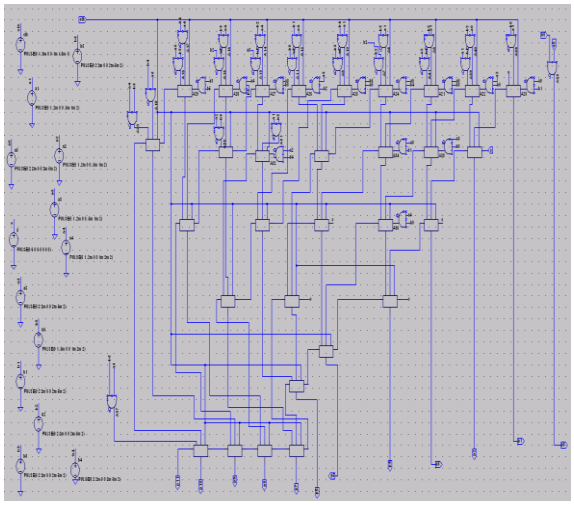

Fig 8. schematic diagram of proposed Wallace tree multiplier.

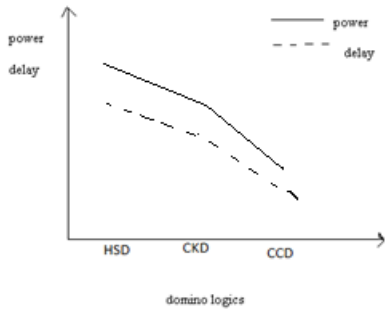

Fig 9: Expected graph of the proposed and conventional results interms of delay and power.

VI. CONCLUSION

A Wallace tree multiplier has to be designed and performance is analysed and compared. The propagation delay and power for the full adder and wallace tree multiplier using CCD logic expected to be less compared with the conventional domino logic.

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