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Low Power Data Acquisition Front End for Wireless Body Sensor Network

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Abstract: Amplifying, Digitizing and compressing the signals from the sensors plays an important role in wireless data transmission. Nyquist sampling of bio– medical signals generates large amount of data from a single sensor which is to be stored and compressed by the processor. The proposed data acquisition platform provides amplification and digitisation at the source itself. Operational Trans conductance Amplifier and 1 bit sigma –delta ADC are designed and simulated using LT Spice.

Keywords: 1-Bit Sigma-Delta ADC, CMOS Technology, LTspice Tool.

I. INTRODUCTION

Wireless body sensor network is a network of wearable or implantable sensors on the human body for continuous long term monitoring of physiological signals such as ECG, EKG, SpO2 and critical biomarkers such as blood glucose. The system could also be designed to allow the physician to remotely access the recorded data, which would allow for a more timely response to any potential warning signs. Such wireless ambulatory monitoring system offer great promise for timely care to the patient at reduced overall costs. It also reduces the burden on the healthcare system by moving health management away from the hospital to the point-of-care at home. For example, for at-risk patients with heart problems, continuous Electrocardiogram (ECG) monitoring can be a more effective and potentially lifesaving approach providing early warning signs to the patient and the Physician.

Wireless body sensor area networks typically consist of multiple sensors that interact with one another, and with a central controller, which is responsible for collection of data from multiple sensors, storage and communication of the data to the physician over the internet. Wireless paradigms are essential for communication to make the system unobtrusive and convenient. However to make the system practical, each sensor node must also be low cost and low power.

II. LITERATURE SURVEY

a) R. R. Harrison and C. Charles in their paper titled "Low- power low-noise CMOS amplifier for neural recording applications " ,[1] presented neural amplifier and schematic of operational trans conductance amplifier

b) M. Trakimas, S. Sonkusale in their paper titled "A 0.8 V asynchronous ADC for energy constrained sensing applications", [2] presented design of an asynchronous Analog-to-Digital converter targeted for low-power sensing applications

c) N. Sayiner, H. V. Sorensen, and T. R. Viswanathan in their paper titled "A NEW SIGNAL ACQUISITION TECHNIQUE **"** ,[5] described A signal acquisition technique that will result in a high resolution high speed Analog to Digital Converter architecture . This technique is based on recording the time instants at which the input signal crosses any of a fixed set of quantization levels and extracting additional information from the non-uniform sample sequence using interpolation methods

d) K. Kozmin, J. Johansson, and J. Delsing in their paper titled "Level- Crossing ADC Performance Evaluation Toward Ultrasound Application",[6] performance evaluation of a level-crossing analog-to-digital converter (ADC) is presented. It is shown that its signal-to-noise ratio (SNR) does not depend on the input-signal amplitude, which results in an almost-flat SNR for amplitudes that fall into the Nyquist criteria for irregular sampling. The influence of the reconstruction procedure on SNR is discussed, and possible limitations due to the comparator and clock on the performance of the ADC are analyzed**.** A level-crossing ADC design example is given for intended use in an ultrasound application with a frequency band from 1 to 10 MHz MATLAB and Cadence simulations, which utilize the data obtained from a real comparator and clock are presented, and the performance of such a level-crossing ADC is compared with a conventional ADC.

III. ANALOG FRONT END AMPLIFIER

A MOS-bipolar pseudo-resistor is used to achieve a very low high-pass cut-off frequency and reduced 1/f noise. A depletion mode PMOS transistor configured as a reverse biased PN diode is added to each input to allow the resistance of the pseudo-resistor to be tuned. By adjusting

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the voltage *Vtune* the bias current of the pseudo-resistors is changed, thus adjusting their AC resistance.

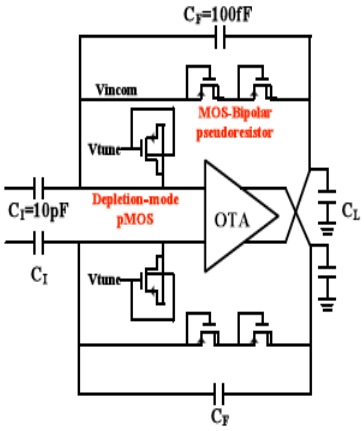

Fig. 1 Bio-potential amplifier with tunable bandwidth

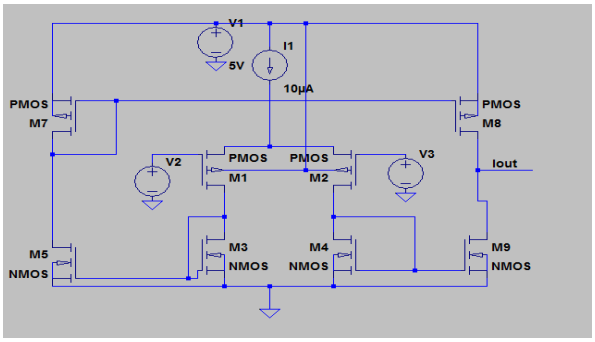

Fig. 2 Schematic of OTA used in neural amplifier

$$I_{out} = g_{m1,2}(V_{in}^{+} - V_{in}^{-}) \quad (1)$$

$$Vout = g_{m1,2}\, R_0\, (V_{in}^{+} - V_{in}^{-}) \quad (2)$$

$$g_{m1,2} = \sqrt{2\beta_{1,2} I_{bias}}/2 \quad (3)$$

$$= \sqrt{\beta_{1,2} I_{bias}}$$

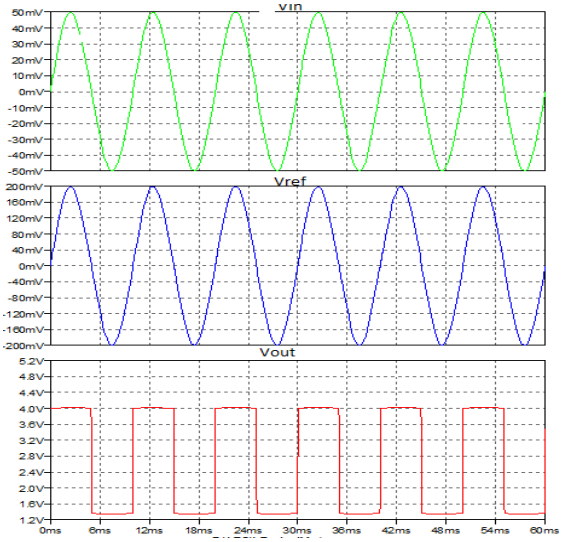

Fig. 3 Input-output waveform of OTA used in neural amplifier

IV. FIRST ORDEAR DELTA-SIGMA MODULATOR

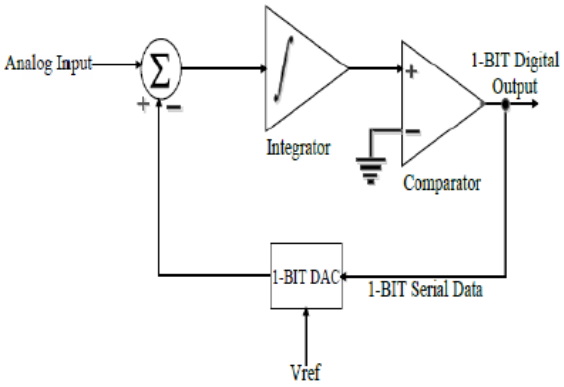

Fig. 4 One-bit Sigma-Delta Modulator

IV. DESIGN OF OPERATIONAL AMPLIFIER

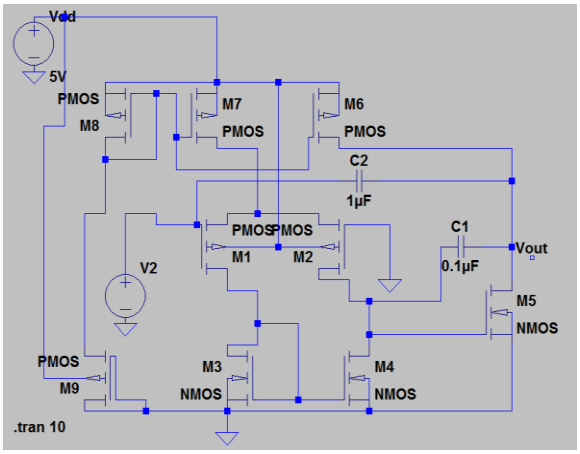

Fig. 5 Schematic of operational amplifier as integrator

Operational Amplifier (Op-amp) is the core part of the Sigma-Delta modulator. It provides a large open loop gain to implement the negative feedback concept as well as let the integrator integrate smoothly. In addition, it has large bandwidth to pass through at least the first two harmonics of input sine wave. The op-amp operates at the clock frequency, since the differences are being integrated over the region of time. Therefore, to effectively pass the signal at the clock frequency the gain bandwidth product of the op-amp must be greater than one. The amplifier used is shown in figure 2. The first stage consists of p-channel differential pair M1-M2 with an n-channel current mirror load M3-M4 and a p-channel tail current source M7, The first stage gives a high differential gain and performs the differential to single ended conversion. This stage gives a good differential gain and also performs the differential to single-ended conversion. The second stage consists of an n-channel common-source amplifier M5 with a p-channel current load M6. The bias of the Op-Amp circuit is provided by M8 and M9 transistors. By using the combination of transistor M8 and M9 which is equivalent to a standard resistor diode (gate tied to drain) combination.

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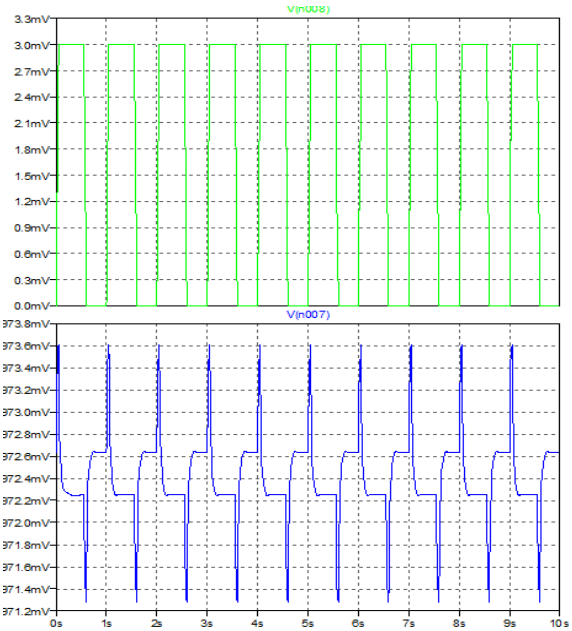

Fig. 6 Input-output waveform of integrator

VI. DESIGN OF COMPARATOR

A comparator acts as the quantizer in the first order modulator. Since the comparator is of 1-Bit it has only two levels either a 1 or a 0. . If the output of the integrator is greater than the reference voltage (Vref) it has to give an output of "1", and if the integrator output is less than reference voltage then the output of the comparator should be "0". A simple comparator performs the required function efficiently. The operational amplifier can be used as a comparator. The only change needed is that the comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail.

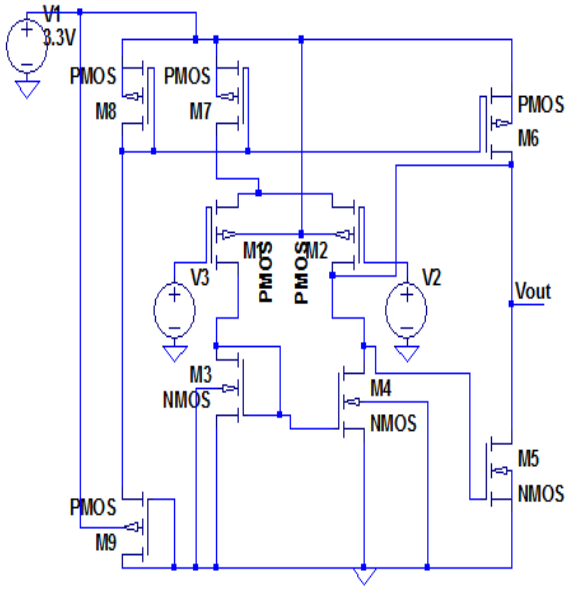

Fig. 7 Schematic of comparator

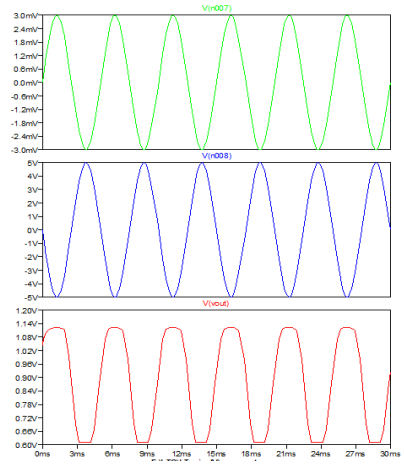

Fig. 8 Input-output waveform of comparator

VII . DESIGN OF 1 BIT DAC

The designed comparator, as a two-stage CMOS operational amplifier, will give an output of 1-bit digital input to the digital to analog converter. A 1- Bit digital-to-analog converter converts the 1-bit digital output of the comparator to the analog signal and this analog signal, fed back to the SC-integrator again. The DAC consists of two transmission gates. The input to each transmission gate is a voltage divided down from the positive and negative 2.5 volt rails which acts as ±Vref signals depending on the 1-Bit digital input signal. The most important component of feedback path is the 1 bit DAC that converts the output digital bit stream to analog value based on a reference voltage. The DAC used is shown in figure 9. The present 1-Bit digital-to-analog converter has two reference voltages a positive reference voltage of +Vref =+2.5v and a negative reference voltage of –Vref.=-2.5v the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted. Frequency response of digital to analog convertor is shown in figure 10. A 1-bit digital to analog converter can be designed using a simple multiplexer circuit, which selects between the +Vref and −Vref signals depending on the 1-bit digital input signal.

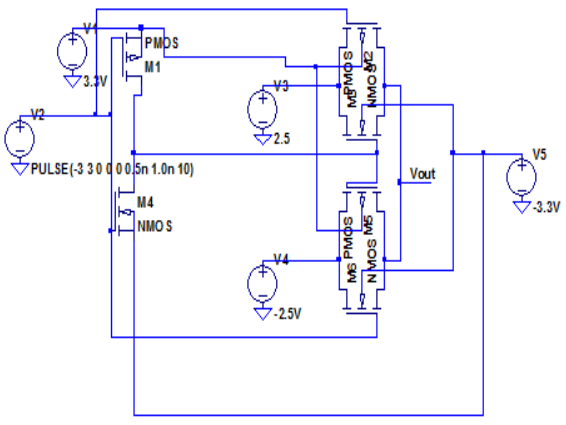

Fig. 9 Schematic of 1 bit DAC

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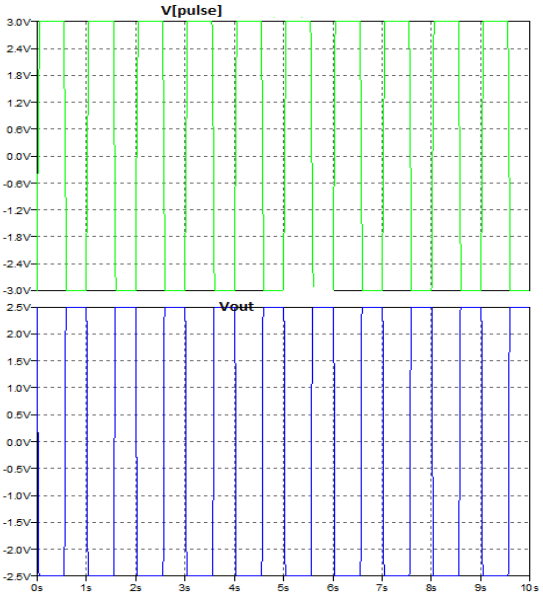

Fig. 10 Input-output waveform of 1 bit DAC

VII. RESULTS AND DISCUSSION

The theoretical results are obtained from LTspice (Linear Technology LTspice IV 4.21b, SPICE Simulator) simulations using SPICE level-1 MOS model parameters. The circuit design of Op-amp, Comparator and DAC for first order Sigma- Delta (Σ-Δ ADC) have been developed and implemented by using 250nm CMOS Technology.

VIII. CONCLUSION

The system is highly suitable for biomedical acquisition in applications such as multi-site neural recording and ECG/EMG recording. The next logical effort in the development of the sensor node is the design of the wireless data transmission. Based on the nature of the data generated, it is expected that impulse based UWB transmitter will be highly suitable.

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