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A novel architecture for a DSCDMA-CI transmitter using cordic and its FPGA Implementation

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Abstract: This paper presents a new approach of designing a DSCDMA-CI Transmitter using the cordic algorithm to generate the carriers whose offset is controlled by the carrier Interferometry (CI) codes. The Architecture thus proposed is reconfigurable, ie the spreading codes can be changed dynamically during the transmission. This design proves better than the traditional DSCDMA transmitters in terms of overall delay, area consumed, complexity and power. The proposed architecture is implemented in SPARTAN 3 FPGA.

Keywords: CORDIC, BPSK modulator, CI codes , FPGA.

I. INTRODUCTION

Direct Sequence Code Division Multiple Access (DSCDMA) is a multiple access scheme which enables users to access the channel over same time and frequency space, however, each user is assigned with a unique code and their data bits are spread using this code before transmission. The user extracts the data bits back from the received signal by de-spreading using the same code[1]. In spread spectrum CDMA technique the transmitted signal is spread over a wide frequency band, more than the minimum bandwidth required to transmit the required information [2].It generates a waveform that appears random to anyone [3] except the intended receiver of the transmitter. The pseudo noise generator is used for this purpose.

The traditional model of DS-CDMA transmitter uses orthogonal codes for spreading in order to reduce the Multiple Access Interference (MAI) but it is seen that these codes lose their orthogonality when signal is transmitted in multipath channel environment. Carrier Interferometry codes, proposed in this paper offers improved performance over traditional orthogonal codes in multipath channel environment. The previous Architecture designs of DSCDMA with real spreading codes uses multiplication of carrier by +1 or -1 depending on the code. However, this architecture is not efficient when spreading codes are complex since complex multiplications are needed for spreading. The spreading using offset generator is based on principle that product of two exponentials is an exponential with angle equal to sum of angle of product components [1].

Thus it offers an alternative low complexity, low power ,more compact DSCDMA transmitter which is also reconfigurable that is the spreading codes can be changed even during the runtime. Since the system generator model consumes more area and time to perform the operation it is therefore implemented using FPGA to reduce the area and power. The rest of this paper is structured as follows. Section II reviews the existing DSCDMA transmitters. Section III gives a brief overview of CORDIC Algorithm Section IV presents the proposed Architecture and Section V shows the results and Section VI concludes this paper.

II. LITERATURE REVIEW

Shibhashis & Sudipta et al. proposed an architecture on "orthogonal minimum correlation spreading code"(OMCSC) in [4]. This architecture was able to provide a large no of spreading codes and simultaneously reduce the effect of MAI in CDMA System. The propose code has been studied and compared with walsh code and kasami code and OMCSC provides lower correlation and better BER performance without sacrificing the number of codes and is less prone to the MAI effect. Tasneem and Ahmed et al. have implemented CDMA communication system with Maximum Length (ML) sequence PN code in [5]. The design is fully reconfigurable, the no of bits & PN sequence can be changed and the transmitter was implemented on FPGA. This has been tested using an arbitrary chosen data stream.

Neenu Joseph & Nirmal Kumar presents the physical layer architecture of SDR in [6]. MC-DS-CDMA system is used as the modulation technique for designing the software defined radio. MC-DS-CDMA is basically a combination of DS-CDMA & OFDM. This technique combines the merits of both (MC) CDMA modulation technique and

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(DS)CDMA technique. The architecture is successful in reducing the bit rate as well as peak power, and speed of the transmission is also increased.

Shrikant and Ingole et al. proposed the multiuser detection also known as joint detection in [7]. The conv-entional detector uses a single-user detection strategy in which each user is detected separately without regard for other users and does not take into account the existence of MAI. Multi-user detection is a better detection. Here, information about multiple users is used jointly to better detect each individual user. Multiuser detection provides better performance compared to the single user detection strategy. Here the reduced multiple interference leads to increased capacity.

Abdulhamid et al. have addressed the problem of Multiuser Detection (MUD) in Direct Sequence/Code Division Multiple Access DS/CDMA communication systems in [8].the sign detector is based on the new algorithm and provides better performance than the maximum likelihood detector as it doesn't involve the exhaustive search to reach the best fitness of the transmitted and received data. generator model consumes more area and time to perform the operation.

III. CORDIC ALGORITHM

CORDIC algorithm is one of the techniques for generate carrier wave in communication system, this algorithm is a unique technique for performing various complex arithmetic functions using shift-add iterations. The algorithm provides low power and area efficient implementation of complex arithmetic operations in many digital signal processing applications.

CORDIC algorithm used for computing a wide range of functions including certain trigonometric, linear, logarithmic and hyperbolic functions. CORDIC is also known as the digit-by-digit method and Volder's algorithm.

It is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available (e.g., simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bit shift and lookup table.

CORDIC is generally faster than other approaches when a hardware multiplier is not available (e.g., a microcontroller), or when the number of gates required to implement the functions it supports should be minimized (e.g., in an FPGA).As the CORDIC algorithm can take into account the speed, accuracy, simplicity and other aspects of performance requirements, it has been widely used in several fields such as the fast Fourier transform (FFT), DTC and other signal processing, image processing, and linear systems, thereby demonstrating the broad application prospects.

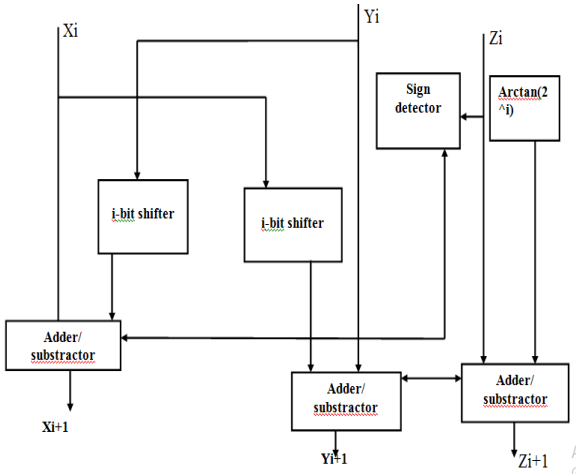

Fig 1: basic cordic processor

The basic CORDIC computations are expressed by the iterative equations at ith step as

$$X_{i+1} = k_i(X_i - m\sigma_i\ 2^{-S(m,i)}Y_i\ )$$
$$Y_{i+1} = k_i(Y_i + \sigma_i\ 2^{-S(m,i)}X_i\ )$$
$$Z_{i+1} = Z_i - \sigma_i\ \ \alpha_{m,i}$$

where i = 0, 1, … , N-1.

m parameter stands for one of the three coordinate systems namely linear, circular and hyperbolic (for m = 0, 1and -1) and S(m, i) is shift sequence having values 0,1, … ,..N-1. Scale factor k_i remains constant for a particular computer if all rotations from 0 to N-1 are completed. Parameter α_i is angle by which a vector is rotated in ith step and is given as :

$$\alpha_i = \tan^{-1} 2^{-i}$$

The parameter σ_i takes two values, -1 and 1. If Z_i, the input angle, is left positive in a particular iteration step then its value is 1 otherwise -1.

The basic block diagram of a cordic processor that is used to generate the carrier is as shown in figure 1. Arctangent values are constant and they are stored in ROM. For the iteration to go from ith stage to(i+1)th, the sign of $Z_i$is predetermined.Adder or substactor is the only computational block in the z-datapath.

It takes three inputs X_i , Y_i, Z_i but it can process only one input at a time.First initialization of all the memory blocks and the shift registers are done with their default values then processing is to be carried out ,its during the processing that the number of times the shifting or how many times the add/substract operation is to be performed will be determined and then based on the arctangent values stored in the memory the sine or cosine of the angle zi is obtained.

If the sign bit is a 1 then add/substactor block adds and the output obtained is the cosine of the angle zi else it is sine

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of the angle. The next iteration can begin only when sign of Z has been determined.

IV. PROPOSED ARCHITECTURE

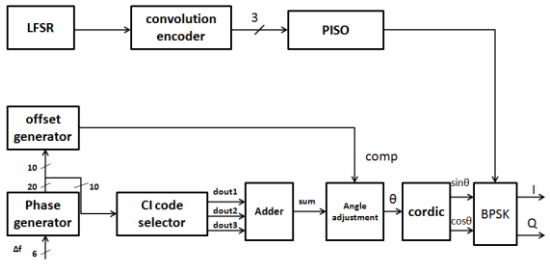

Fig 2: DSCDMA transmitter using BPSK modulator

The figure 2 shows the proposed architecture of DSCDMA transmitter. The transmitter consists of 7 major blocks namely: LFSR, convolution encoder, BPSK modulator, Phase accumulator, phase offset generator ,code selector and cordic block. In the next subsections each of these blocks are discussed in detail.

A. LFSR:
To generate randomized binary data stream a linear feedback shift register (LFSR) is used. An LFSR is a shift register whose input bit is a linear combination of its previous state, by using this LFSR we generate pseudo random numbers. The LFSR sequence goes through 2m - 1 states, where m is the number of registers in LFSR. The state of all zeros is not allowed as the LFSR would be locked in this state.

B. Convolution encoder:
Convolution encoder of 1/3 rate is used .The working principle of convolution encoder is that the encoder performs a convolution of the input stream with encoder's impulse response. In this work, a non systematic non-recursive rate 1/3 convolutional code with constraint length 7 is used. It consist of a clock divider and a data generator. For each data bit as input convolution encoder produces 3 encoded bits serially at the output.

C. BPSK modulator:
A BPSK modulator is used to find whether the characteristics of the message signal is suitable for the transmission through the channel or not. Binary Phase Shift Keying (BPSK), a phase shift of 0 is given to the carrier if the message bit is 1; otherwise, a phase shift of 180 is given. The working of modulator with the multiplexer can be enlisted in following steps:

D. Phase accumulator:
Phase accumulator is nothing but a counter.It consists of a frequency controller and an accumulator. Input to the phase accumulator is a frequency control word. When clocked the phase accumulator creates a modulo 2^N saw-tooth waveform which is then given to the adder which adds it together with the CI code selector output to form the phase angle for the cordic.

E. phase offset generator
The offset generator generates phase offset equivalent to the spreading bit. It's same as the phase generator except that it has the complemented values.

F. Code selector:
Code selector is used to add configurability to the design and verify waveforms for various codes, The block consists of gain blocks, multiplexer and selection input. The selection input of multiplexer can be used to select different user spreading codes. The selection input to the multiplexer can be used to change the spreading code dynamically during runtime.

G. PISO:
The data from the encoder is 3 bits therefore a parallel in serial out(PISO) is used to convert the data which is of 3 bits into a single bit.

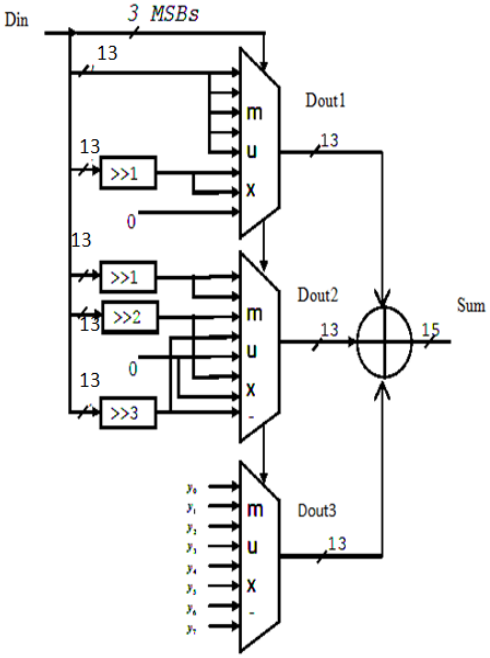

Fig 3: Carrier Interferometry (CI) code selector

The above figure shows the internal architecture of the CI Code selector.

H. CORDIC block:
The sum of output of code selector and phase generator is the angle of the carrier. However, to ensure that the angle lies within the domain of convergence of CORDIC this block is used. The angle of the carrier is given as the input to the cordic block, for angle adjustment which in turn generates the sine and the cosine output which is given to the multiplexer along with the message bit from the convolution encoder. Then the message signal is modulated using the BPSK modulator.

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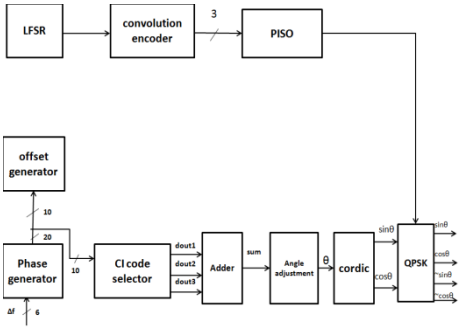

Fig 4: DSCDMA transmitter using QPSK modulator

The fig 4 shows the DSCDMA transmitter that makes use of QPSK modulation the rest of the blocks are the same as that of the system designed in fig 2.The QPSK modulator generates a sinθ for 00,cosine for 01,~sinθ for 10 and ~cosθ for 11.

The summary of working of transmitter is given below:

- LFSR acts as a data source to the convolution encoder and the encoder encodes the data at 1/3 rate. The encoded output is given as the message input to the BPSK modulator through a parallel in serial out (PISO) which will generate the serial output
- The phase generator is given with the frequency offset of 6 bits which produces the output of 20 bits, the 10 bits of the phase generator is given to the offset generator
- The offset generator is similar to the phase generator except that it complements the values.
- The remaining 10 bits is given to the CI code selector, where the 3 MSBs are used as the select line to the Muxes, the rest 7 bits are appended with 6 zeroes , 3 zeroes in LSB and 3 in MSB and then given as the input to the multiplexers.
- The CI code selector has three muxes whose outputs are dout1, dout2, dout3 each 13 bits which is then added together using an adder and two zeros are added to the MSB to obtain a sum of 15 bits.
- The sum is then given to the angle adjustment block which depending on the select line comp will either complement the sum if it is a 1 else the sum will be sent as it is to the output.
- The output of the adjustment block is the angle θ which is given to the cordic processor to obtain the sinθ & cosθ which are given as the carrier waves to the BPSK modulator.
- The modulator will select the in phase sine wave if the message bit is 1 else a quadrature phase cosine wave in case of the BPSK modulator and if it's the QPSK modulator then the data_out is a sinθ for 00,cosine for 01,~sinθ for 10 and ~cosθ for 11.

V. RESULTS

The DSCDMA/CI transmitter using BPSK Modulator and QPSK Modulator is designed and the waveforms obtained on simulation is as shown below.

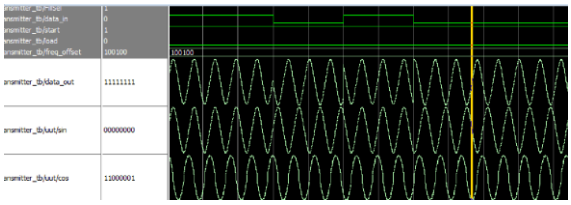

Fig 5: Waveform generated for transmitter using BPSK modulator

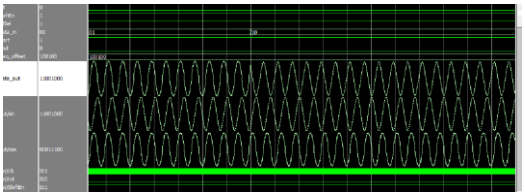

Fig 6: Waveform generated for transmitter using QPSK modulator

VI. CONCLUSION

An architecture for DS-CDMA/CI transmitter using Cordic Algorithm. As the system generator design model takes more area and time to perform the operation, it is therefore implemented using the FPGA to reduce the area and power. The architecture uses CORDIC block to generate carrier and to avoid use of complex multiplications the phase offset equivalent to spreading code is added to the phase generator output. Code selector block adds runtime re-configurability to the model. Then these modules are implemented in SPARTAN3 FPGA by using Xilinx ISE 13.4 and simulated in modelsim 6.3f. The Chipscope pro Analyzer is used to view the execution results of FPGA.

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