Design and Implementation of SDR Transceiver Architecture on FPGA

Shreevani. C[1], Ashoka. A[2], Praveen. J[3], Raghavendra Rao. A[4]

M.Tech, 2nd year, VLSI Design and Embedded Systems, ECE Dept., A.I.E.T, Mijar, Moodbidri, Karnataka, India[1]

Assistant Professor, ECE Department, A.I.E.T, Mijar, Moodbidri, Karnataka, India[2]

Senior Associate Professor, ECE Department, A.I.E.T, Mijar, Moodbidri, Karnataka, India[3, 4]

Abstract: Usage of Software-Defined Radio (SDR) in digital communication systems can easily cater to sophisticated coding and modulation techniques, to meet the ever-increasing requirements of the wireless communication industry. Future generation of wireless communications will meet the requirements of Software Radio technology as it would provide the state-of-art design to complex radio designs. Software-defined radios are configurable devices in which the components can be reprogrammed to emulate various functionalities like data rate, modulation, filtering etc. Field programmable architectures provide a suitable platform to achieve such run-time reconfigurations of the components of the radio. Software defined radios are highly configurable that provide the technology for realizing the rapidly expanding third and future generation digital wireless communication infrastructure. There are a number of silicon alternatives available for implementing the various functions in a SDR, field programmable gate arrays (FPGAs) are an attractive option for many of these tasks for reasons of performance, power consumption and flexibility. The aim of this project is to study and understand SDR using Xilinx [1].

Keywords: QPSK, Power efficiency, Spectral efficiency, Synchronization.

I. INTRODUCTION

SDR is a process in which the components like baseband signal, carrier frequency, signal bandwidth, modulation techniques, filtering, transmitter and receiver are implemented by software. Currently with the existing technology and developmental tools, SDR is able to implement complex communication systems comprising of many waveforms at many frequencies. The basic notion behind is to seek the feasibility of getting the software as close to the antenna as possible, thus solving hardware problems by software. The advantage of this approach is that the equipment is more versatile and cost-effective. This technique illustrates the design and implementation of low frequency trans-receiver based on SDR legacy. The low frequency trans-receiver based on FPGA provides flexibility in implementation and simple to upgrade. This practical approach has been adopted to implement the low frequency trans-receiver. Similarly, DDS is relatively a new technology of frequency synthesis and is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems [1].

Software Defined Radio (SDR) is a radio communication system where components that have been typically implemented on hardware are instead implemented by means of software on a personal computer or embedded system. While the Software defined radio is not new concept, the rapidly evolving capabilities of digital electronics render practical many processes which used to be only theoretically possible. A software defined radio (SDR) allows for digital communication system to easily adopt more sophisticated coding and modulation techniques, which is extremely important in meeting the ever increasing demands of the wireless communication [7]. The signals with high frequency can be transmitted in radio communication system. On one hand, only the signal with high frequency can be transmitted over a long distance; on the other hand, the height of the antenna has a strong relationship with the signal frequency. The lower the frequency the higher the antenna is. Thus to transmit low frequency signal may require a very high antenna which ever cannot be made out. Whenever the signal with low frequency needs to be transmitted it is necessary and important to modulate it to a high frequency signal. Only in this way can the signal be transmitted in the radio communication system. Modulation techniques are used in SDR. Modulation is a process in which some characteristics of the carrier wave are varied with respect to modulated signal.

Three major kinds of modulation technologies are used in radio communication system. They are Amplitude-Shift Keying (ASK), Frequency-Shift Keying (FSK) and Phase-Shift Keying (PSK). In recent years BPSK and QPSK are being used. BPSK stands for Binary Phase Keying which is the simplest PSK. In BPSK the carrier signals phase varies between two values according to the modulating signal. To improve efficiency QPSK modulation is being used. Quadrature Phase Shift keying is another phase shift modulation method which is little more complex than BPSK. It has twice bandwidth efficiency of BPSK [3].

II.   LITERATURE REVIEW

The term "digital receiver" was coined in 1970 by a researcher. A laboratory called the Gold Room in California created a software baseband analysis tool called Midas which of course was software defined. The term "software radio" was coined in 1984 by a team at the Garland, Texas Division of E-Systems. A 'Software Radio Proof-of-Concept' laboratory was developed there that popularized Software Radio within various government agencies. This 1984 Software Radio was a digital baseband receiver that provided programmable interference cancellation and demodulation for broadband signals, typically with thousands of adaptive filter taps, using multiple array processors accessing shared memory. In 1991, Joe Mitola independently reinvented the term software radio for a plan to build a GSM base station that would combine Ferdensi's digital receiver with E-Systems Melpar's digitally controlled communications jammers for a true software-based transceiver.

The first major push for the development of the SDRs is made through US military paper named SpeakEasy. The primary goal of the SpeakEasy paper was to use programmable processing to emulate more than 10 existing military radios, operating in frequency bands between 2 and 2000MHz. another design goal was to be able to easily incorporate new coding and modulation standards in the future, so that military communications can keep pace with advances in coding and modulation techniques.

SpeakEasy phase I
From 1992 to 1995, the goal was to produce a radio for the U.S. Army that could operate from 2 MHz to 2 GHz, and operate with ground force radios, Air Force radios, Naval Radios and satellites.

SpeakEasy Phase II
The goal was to get a more quickly reconfigurable architecture in open software architecture; with cross channel connectivity (the radio can bridge different radio protocols). The secondary goals were to make it smaller, weigh less and cheaper.

Chris dick et al [2], proposed the carrier synchronization in SDRs using FPGA based signal processors. The carrier synchronization in SDRs provided overview of carrier recovery techniques for QPSK and QAM modulation schemes on the design and FPGA. It examines maximum likelihood carrier phase synchronization for QAM (Quadrature amplitude modulation) based SDR personalities. The FPGA device utilization and performance for a carrier recovery circuit using a look-up table approach are presented. The most complex component in the loop is the phase detector. Since the phase of QPSK or QAM signals is data dependent, the phase detector must strip the modulation from the received signal and produce a signal proportional to the phase difference between the local generated quadrature carriers and those of the received signal. The implementation of the high-performance digital communication systems has been made possible by advances in semiconductor process technology in the form of application specific standard parts, full custom silicon chips, instruction set based digital signal processors (DSPs) and high performance general-purpose processors (GPP). The phase error is computed by comparing the phase difference between the received signal and the closest constellation point.

Asraf Mohammed Moubark et al [3], proposed that modulation is a key feature commonly used in wireless communication for data transmission and to minimize antenna design. QPSK (Quadrature Phase Shift Keying) is one type of digital modulation technique used to transfer the baseband data wirelessly in much efficient way compare to other modulation techniques. Conventional QPSK modulator operates by separation of baseband data into i and q phases and then add them to produce QPSK signal. The process of generating sine and cosine carrier wave to produce i and q phases consume high power. For better efficiency in power consumption and area utilization, 2 new types of QPSK modulator proposed. The proposed method will eliminate the generation of 2 phases and will produce the QPSK output based on stored data in RAM.

Shriram K Vasudevan et al [4], developed a model of a Software defined Radio using SIMULINK tool to implement the IEEE 802.11 standard and the Bluetooth standard. The main aim was to build various protocols for WLAN and the Bluetooth standards and to demonstrate their functionality. This includes implementation of IEEE 802.11a standard for the WLAN and basic core protocols for the Bluetooth. To develop a model of a Software Defined Radio which supports the IEEE 802.11a standard and Bluetooth standard using the SIMULINK tool, to implement all the main protocol stacks for WLAN and Bluetooth Protocols and verify their functionality, to transmit the data as frames using the format specified for the standard, to compress the binary data using source coding algorithm and also encode the data for Forward Error Correction (FEC). to modulate the binary stream of data using the BPSK modulation for WLAN mode which supports the basic transfer mode with 6 Mbps speed, for the Bluetooth standard the basic modulation scheme used is GPSK and Frequency hopping spread spectrum is used, to implement algorithm for WLAN security and also CRC-16 for protecting the integrity of the data, to implement point to point communication and data transfer for the Bluetooth standard, to implement CSMA/CA technique and also implement different basic functions such as packet routing, Authentication, Request to transmit etc. for the WLAN standard.

Ziyi feng et al [5], from university of applied sciences implemented software defined radio using MATLAB to

design a radio communication system in audio band using audio devices such as a sound card. The idea of SDR is to use ultra-high speed sampling and ADC/DAC modules directly measure the received radio signal and decode whatever it contains. The aim was to study and understand SDR using MATLAB in audio frequency band. Both analog and digital modulation and demodulation methods are studied. This will employ one desktop PC with MATLAB installed and simulates the radio communication process. Two Matlab sessions are executed at the same time, one as transmitter, and the other as receiver. When the project works, the signal is produced in transmitter and transmitted as sound after modulated. Then the receiver will receive the signal by recording it. The information can be obtained after demodulation.

Anton S. Rodriguez et al [6], proposed that software-defined radios (SDR) provide a versatile wireless communication solution for a wide range of applications, including cellular telephones, global positioning systems, and military grade communications. The SDR is applicable in nearly any wireless communication system and when implemented on a Field Programmable Gate Array. The SDR is a very cost-effective system in many ways. Since all hardware is physically programmed using software, re-design becomes relatively simple. Rather than discarding old hardware, the SDR is simply reprogrammed, updated and loaded back onto the FPGA, saving both time and money. The SDR also provides a capability for high quality communication without a need for expensive broadcasting equipment. In addition to its cost benefits, the SDR is also a very powerful and flexible system. In wireless communication, this means faster data rates and highly configurable modulation technology. Quadrature phase shift keying (QPSK) is a modulation scheme which sends a pair of bits per symbol, increasing data rate by a factor of two. A typical problem in QPSK and in wireless communication is carrier synchronization, or the synchronization of the oscillator at the receiver with the oscillator at the transmitter. In order to do so, a phase-locked loop circuit must be appended to the receiver. This provides the local oscillator at the receiver with a frequency adjustment. However, once this correction is made, a static phase error called phase ambiguity will still exist.

III. QPSK THEORY

Quadrature phase shift keying (QPSK) is a digital modulation scheme where each symbol is represented by a pair of bits, increasing data rate by a factor of two in a given bandwidth. Higher modulation schemes, such as 8PSK and 16-PSK, sends three or four of bits per symbol to increase data rates even further. A typical concern in wireless communication using QPSK modulation is carrier synchronization at the receiver and hence requires a phase lock loop based carrier recovery technique at the receiver. For transmission to and from a satellite, the information

(baseband digital signal) must be modulated onto a microwave carrier. In general, the digital baseband signals may be multi-level (M-ary), requiring multilevel modulation methods. With QPSK, the binary data is converted into 2-bit symbols I, Q which are then used to phase modulate the carrier. Since four combinations containing 2 bits are possible from binary information (logical 1 s and 0s), the carrier phase can be shifted to one of the four states and transmitted. The mathematical representation of the transmitted signal, s(t) can be written as $s(t)=I(t)\cos(2\pi fot)-Q(t)\sin(2\pi fot)=\cos(2\pi fot+\phi(t))$ (2)

Here I,Q $\in$ {1/√2, -1/√2} and fo denotes the carrier frequency and the vectors I, Q carry one bit information each $2\pi fct$.
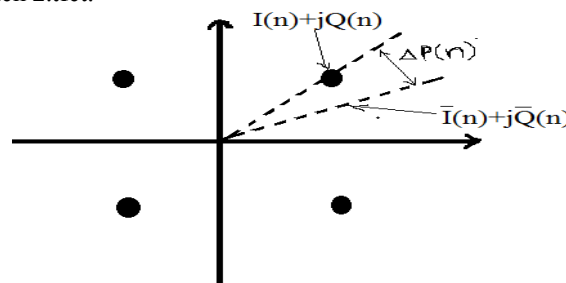

Fig:1 QPSK constellation grid

The received signal is demodulated and the decoded data can be represented as constellation diagram on an x-y plane in terms of symbols at 45, 135, 225 and 315 degrees respectively. Each symbol in the constellation represents two bits of information that are decoded based on their position in the constellation. Performance of any radio system depends on the efficiency of the modulation scheme used. The two most important factors that decide the overall efficiency of the modulation scheme are power efficiency and bandwidth efficiency. Power efficiency is the ability of the modulation technique to preserve the quality (e.g. BER) of the signal with minimal signal power. It is defined as the ratio of signal energy per bit to noise spectral density (Eb/No) required to achieve a particular BER. Bandwidth efficiency is the ability of the modulation technique to transfer more data at the given bandwidth, which decides the symbol/channel capacity. It is defined as the ratio of data rate in bits per second to allocated bandwidth in Hertz (R/B). There exists a fundamental trade off in any communication systems between the power efficiency and bandwidth efficiency as one can be achieved only at the expense of the other. We can represent QPSK signals by:

$$s(t)=\frac{1}{\sqrt{2}}d_I(t)\cos(2\pi f_ct)+\frac{1}{\sqrt{2}}d_Q(t)\sin(2\pi f_ct) \qquad (1)$$

Two BPSK modulated signals combined together to represent a QPSK signal by using two orthogonal carrier signals. One is given by cos (2πfct) and the other is given by Sin (2π fct).

IV.   DESIGN OF QPSK TRANSCEIVER

The low frequency QPSK Transmitter-Receiver design is illustrated in Fig: 2.QPSK modulation will be done for the input. The output of the QPSK modulation will be In-phase and Quadrature phases. Those two signals will be given to the mixer. Mixer is a combination of Multiplier, DFS and delay register. DFS will generate the carrier signals. Sine and cosine sinusoidal signals will be given to multiplier. The multiplier will combine the signals from DFS and modulator and generates I and Q signals. The adder will add the real and imaginary functions respectively. The output of the transmitter will be given as input to the receiver. The components of the transmitter were also be used in receiver. To extract information in the receiver we need to add carrier by using DFS. I and Q signals which are generated will be combined using adder. The output of the receiver will be demodulated using QPSK demodulator. The input of the transmitter with the output of the receiver will be matched.
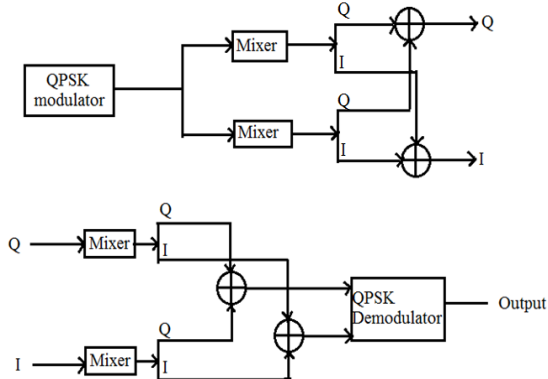

Fig:2 QPSK Transmitter and Receiver

Modulation is a key factor commonly used in wireless communication for data transmission. QPSK is one type of digital modulation technique used to transfer data in much efficient way compared to other modulation technique. QPSK is formed from two separate BPSK which combined together. The data transmission is twice than BPSK. The symbol rate for QPSK is also two times the bit rate.

Digital frequency synthesizer consists of phase accumulator and a phase to amplitude convertor. Phase accumulator consists of frequency register to store digital phase increment word followed by full adder and a phase register. For every clock along with the delay phase accumulator will increment the value. Complementing is also done after accumulation. Phase to sine amplitude convertor is used to approximate the first quadrant of sine function with equal eight length piecewise linear system. The main goal is to maintain low system complexity and reduce power consumption and chip size.

V.   DIGITAL FREQUENCY SYNTHESIZER

Digital Frequency Synthesizer (DFS) is used in communication system to generate a sampled sinusoidal carrier wave. The major advantages of DFS method is that precisely and rapidly manipulate its output frequency, phase and amplitude under the control of a DSP.

DFS has the ability to tune with extremely fine frequency and phase resolution and to rapidly hop between the different frequencies. Modulation is carried out using DFS, which has multiplier less structure, utilizes less resource on FPGA and in demodulation same architecture is used to obtain the digital data back. It consists of a phase accumulator and a phase to amplitude converter. a hardware-optimized phase-to-sine amplitude converter used to approximate the first quadrant of the sine function. The main goal is to maintain low system complexity and reduce power consumption and chip area requirements. The second aim is to achieve a specified spectral purity.
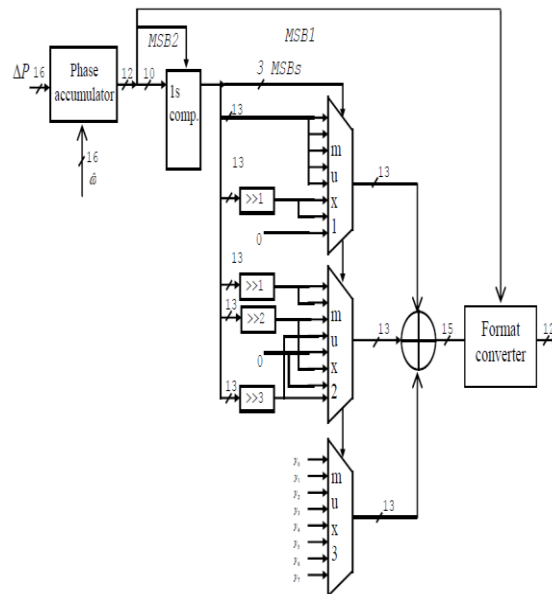

Fig: 3 DFS Architecture

Complete DFS architecture is shown in Fig 3. The phase to sine amplitude converter block includes a 1's complement to exploit quarter wave symmetry. This architecture is significantly less complex. It does not include a ROM, no multipliers or squaring circuits are required. To simplify the control circuitry equal length segments are used. Only three integers need to be added and multiplexers. The phase accumulator is of 20 bits wide, truncated to 12 bits. The two MSBs are used for quadrant symmetry. Segment is identified by the next three bits. The remaining seven bits identify different sub-angles. The two upper multiplexers shift these remaining seven bits according to the slopes. The output from the multiplexers is of 13 bits wide, to account for the whole dynamic range of possible values. The three-operand adder sums the multiplexer outputs together and rounds the result to 7 bits.

Architecture for digital frequency synthesizer is presented. DFS architecture can be used to perform modulation &

demodulation in communication system. DFS has the ability to tune with extremely fine frequency and phase resolution and to rapidly hop between the frequencies [5].
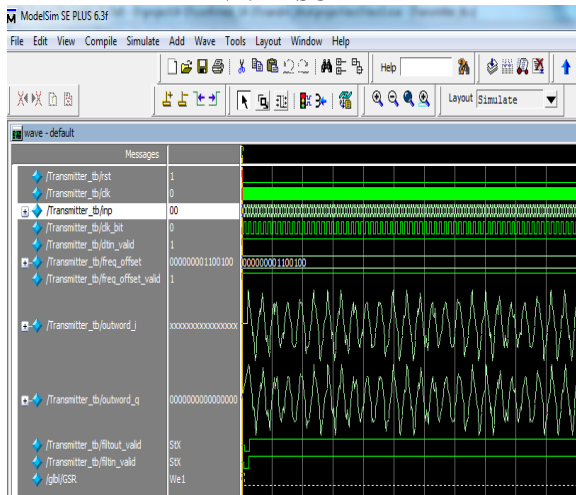
VI. RESULT

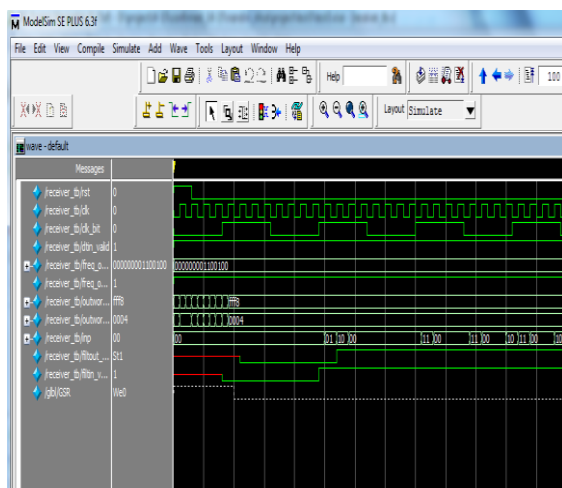Fig: 4 Simulation result of SDR Transmitter

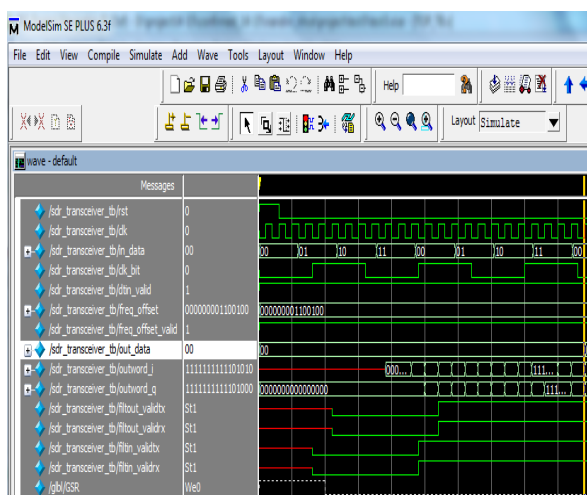Fig: 5 Simulation result of SDR Receiver.

Fig: 6 Simulation result of SDR Transceiver

VII. CONCLUSION

SDR of low frequency trans-receiver was successfully implemented on a single FPGA chip. The measured results show that transmitter input matches with the receiver output. Also it provides a low cost, low power solution. FPGA implementation may further provide flexibility in customizing the design for different data rates, Modulation types, Carrier Frequency, Filter types etc making the design effectively reconfigurable. Any change in the requirement specifications, the SDR is reprogrammed, updated and loaded back onto the FPGA, saving both cost and time instead of discarding old hardware. The SDR is also emerging as a popular platform. Software defined radios constitutes a versatile platform for wireless communication solutions like cellular, global positioning systems and military grade communications. Future work would involve usage of error coding / decoding, carrier recovery algorithms, M-ary PSK modulation etc to deliver a scalable customized design.

REFERENCES

[1] Shahana K, Ravi Kumar Gupta, K S Parikh,"SDR implementation of low frequency trans-receiver on FPGA".

[2] Chris Dick, Fred Harris, and Michael Rice, " FPGA implementation of carrier synchronization for QAM receivers", Journal of VLSI Signal Processing, Kluwer academic publishers, Netherland, 2004.

[3] Asraf Mohammed Moubark, Mohd Alauddin Mohd Ali, "Simple QPSK Modulator Implemented in Virtex 6 FPGA Board for Satellite Ground Station".

[4] Shriram K Vasudevan, Sivaraman R, Z. C. Alex "Software Defined Radio Implementation", 2010.

[5] Anupama B.R, M C Chandrashekhar, "Implementation of digital frequency synthesizer in digital communication system using FPGA".

[6] Anton. S. Rodriguez, Michael. C. Mensinger, "Software Defined Radio Using Xilinx".

[7] Dennis Roddy, Satellite Communications.

[8] Vinod Kumar,Venkat Reddy Gari, "FPGA-based QPSK transceiver design", Technical Report, Department of Electronics and Computer Engineering 2008.

[9] Divya Jain, Sandhya Gautam, Teena Sakla, "Implementation of Digital QPSK Modulator by Using VHDL/MATLAB", International Journal of Engineering and Technology, 2010.

[10] Wenmiao Song, Qiongqiong Yao, "Design and implement of QPSK modem based on FPGA", 3rd IEEE International Conference on Computer Science and Information Technology (ICCSIT), 2010.