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Design of Low Power Flip-Flop with Signal Feed Through Scheme for Counter Design Applications

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Abstract*:* A low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using cadence virtuoso CMOS 180-nm technology, the proposed design outperforms the conventional P-FF design. The proposed design features the best power-delay-product performance in both implicit and explicit type flip flops under comparison. Counters can be designed using such flip flop. As a result power consumption is reduced compared to conventional methods. In this paper, a low power explicit pulse triggered flip flop is discussed as a proper choice of low power applications and comparison with other flip flop architectures.

Keywords: Flip-flop (FF), low power, pulse-triggered, signal feed through scheme.

I. INTRODUCTION

The increasing significance of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density Very Large Scale Integration (VLSI) chips have led to rapid and innovative developments in low-power design during the recent years. Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage.

If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and characteristic a zero or even negative setup time.

Depending on the method of pulse generation, P-FF designs can be classified as implicit and explicit.

In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated.

In an explicit-type P-FF, the designs of pulse generator and latch are separate.

II. CONVENTIONAL APPROACHES

A. Explicit Pulse Data Close To Output(ep-DCO)

A typical explicit P-FF design, named data-close to-output (ep-DCO) contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design as shown in fig. 1.

In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters.

This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

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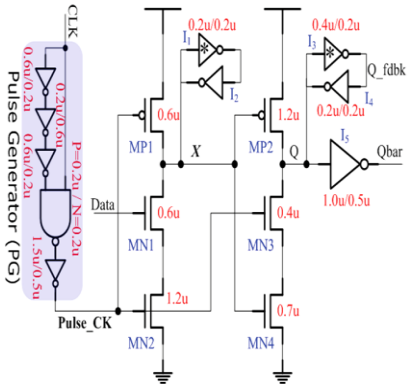

Fig.1.ep-DCO

B. Conditional discharge flip flop(CDFF)

Fig.2 shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is in use so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node *X* is simplified and consists of an inverter plus a pull-up pMOS transistor only.

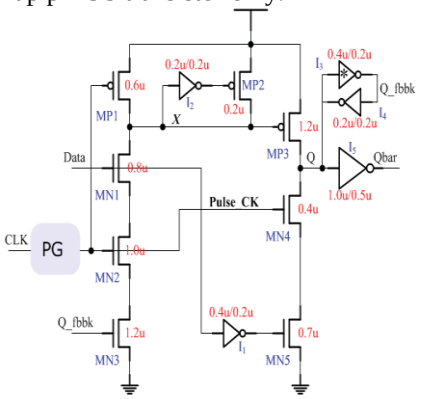

Fig.2 CDFF

C. Static conditional discharge(SCDFF)

Fig. 3 shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node *X* is thus free from periodical precharges. It encounters a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3.

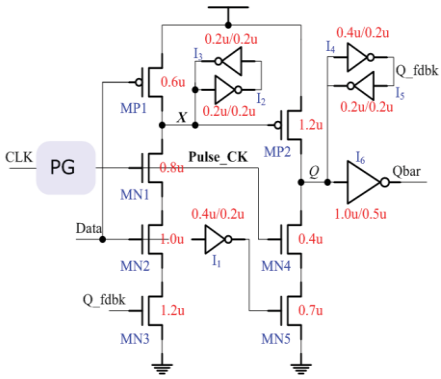

Fig.2.3:SCDFF

D. Modified Hybrid Latch Flip Flop(MHLFF)

To overcome the delay which occurred in CDFF and for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flipflop (MHLFF) shown in fig. 4 also uses a static latch. The keeper logic at node *X* is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node *X* when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node *X* is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT*)* is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power .

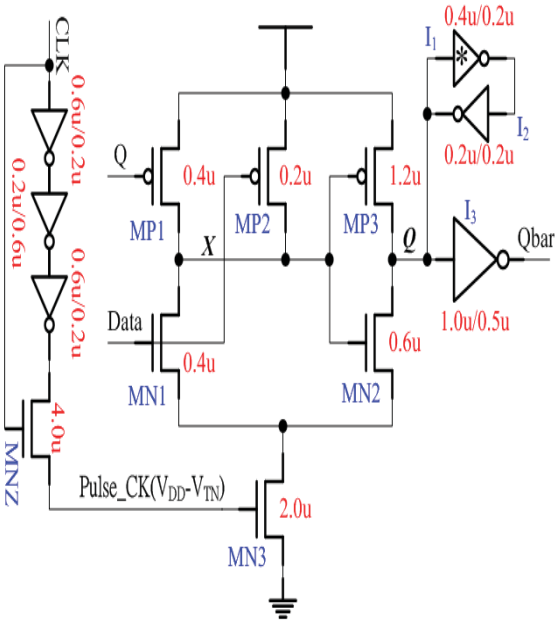

Fig.4 MHLFF

E. Single Ended Conditional Capture Energy Recovery(SCCR)

Fig.2.5 shows a refined low power P-FF design named single ended conditional capture energy recovery (SCCER) using a conditional discharged technique. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X [5]. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X , an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and

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a longer delay from the delay inverter I1 to widen the discharge pulse width.

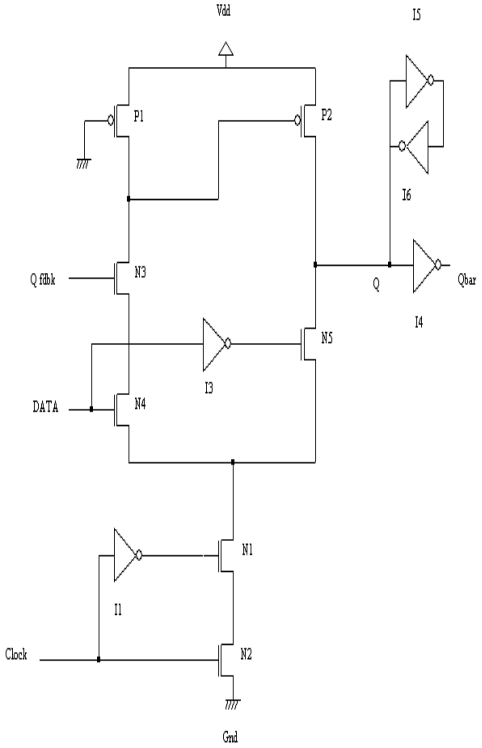

Fig.5 SCCR

III. PROPOSED DESIGN

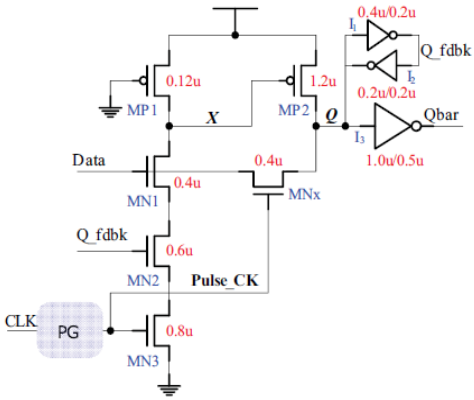

Fig.6 Proposed circuit

The circuits reviewed in Section II,they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig.6 the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node . Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter.

The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors. The principles of FF operations of the proposed design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node *X* is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high. this corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened.

Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. When a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the

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speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

IV. SIMULATION RESULTS

A. *Explicit Pulse Data Close To Output(ep-DCO)*

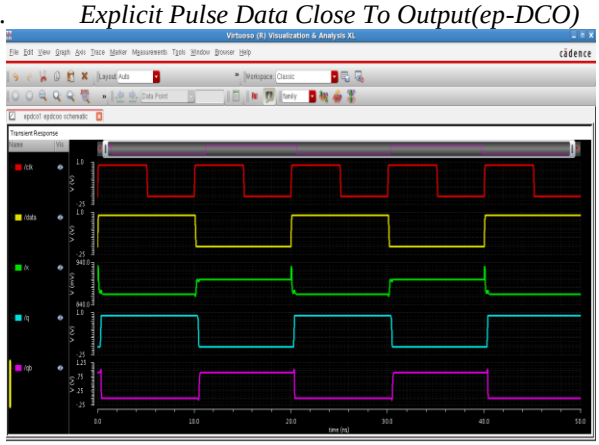

Fig .7 Output waveform of ep-DCO

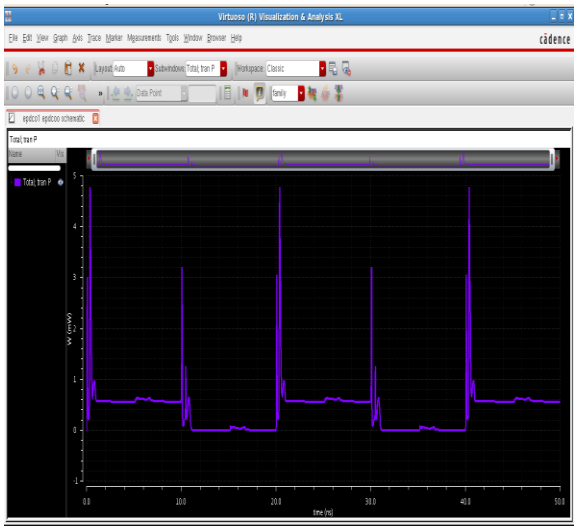

Fig.8 Power plot of ep-DCO

B. *Conditional discharge flip flop(CDFF)*

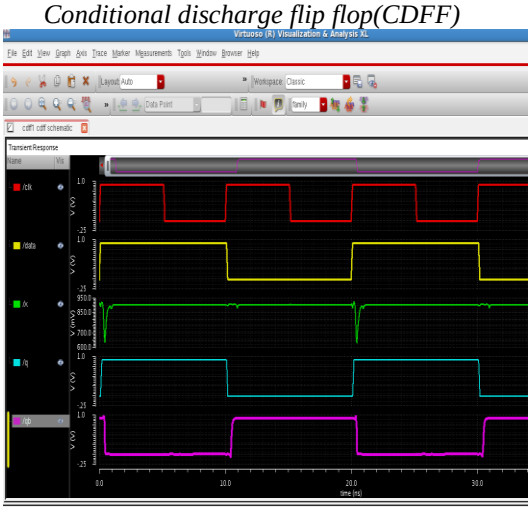

Fig .9 Output waveform of CDFF

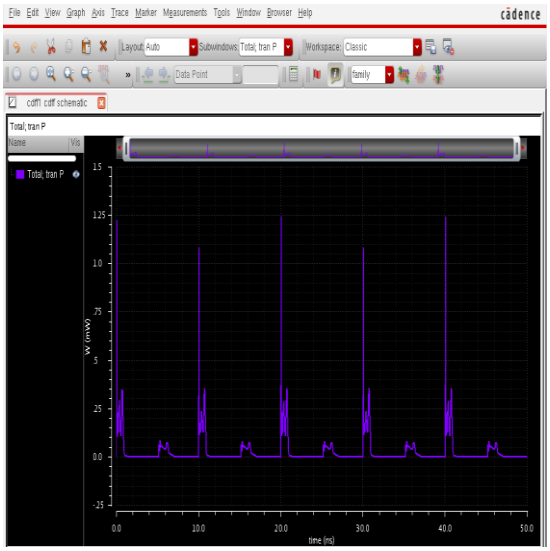

Fig.10 Power plot of CDFF

C. *Static conditional discharge(SCDFF)*

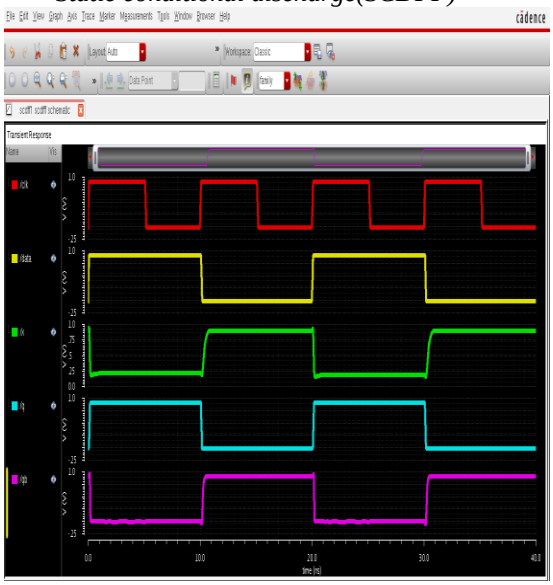

Fig .11 Output waveform of SCDFF

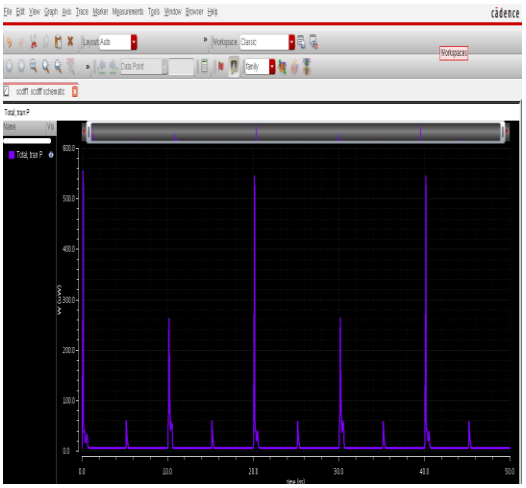

Fig.12 Power plot of SCDFF

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D. Modified Hybrid Latch Flip Flop(MHLFF)

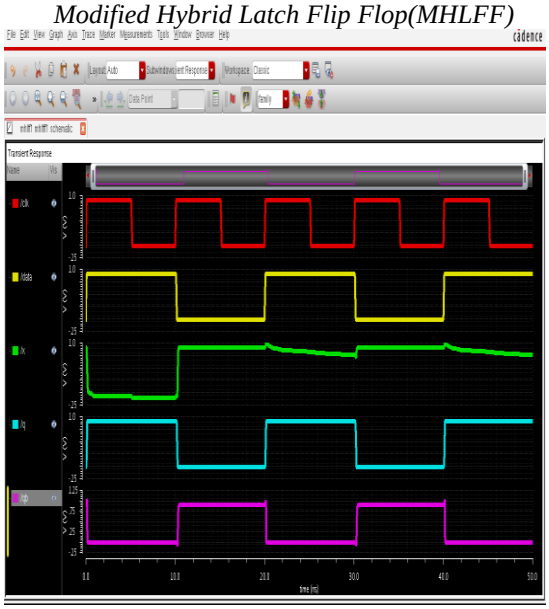

Fig .13 Output waveform of MHLFF

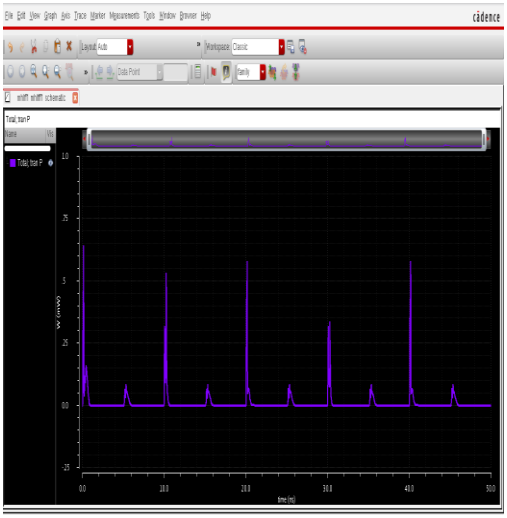

Fig.14 Power plot of MHLFF

E. Single Ended Conditional Capture Energy Recovery (SCCR)

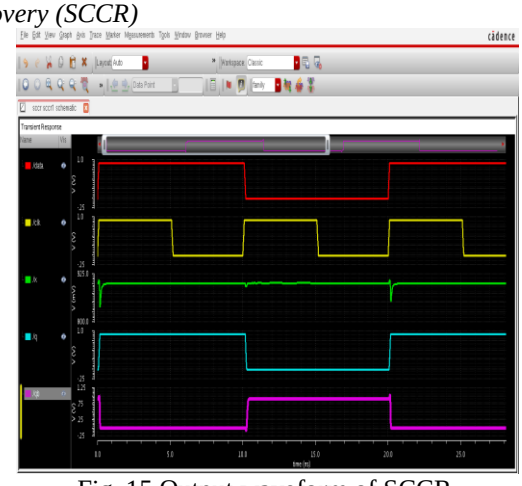

Fig .15 Output waveform of SCCR

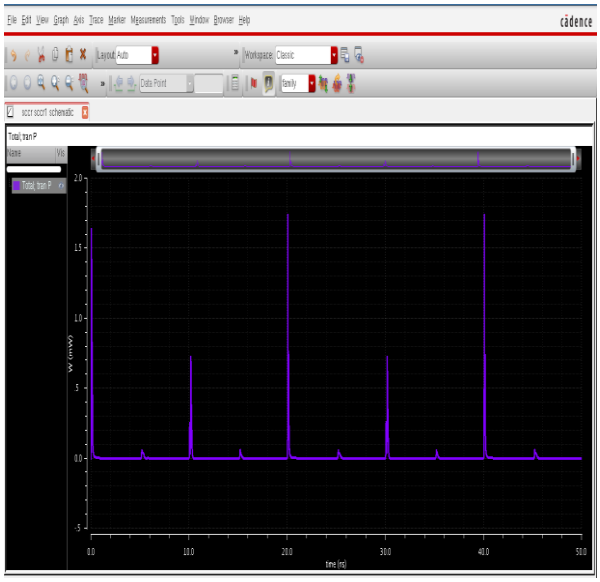

Fig.16 Power plot of SCCR

F. Proposed circuit

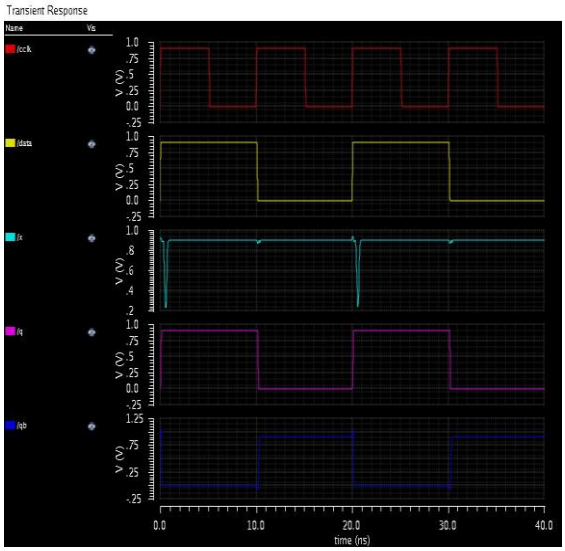

Fig .17 Output waveform of proposed design

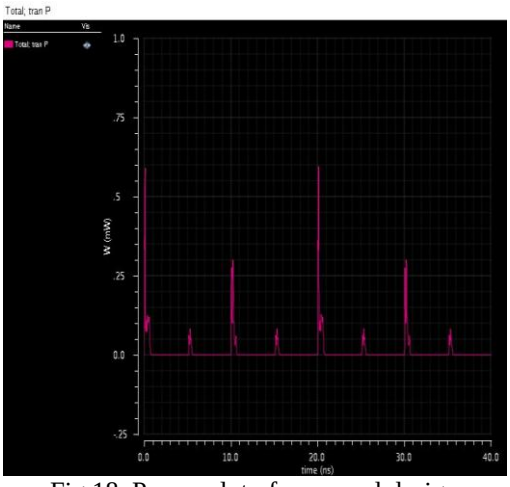

Fig.18 Power plot of proposed design

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G. Power delay analysis

Table I:Power and delay

Flip flop	Transmitted power(μW)	Delay(Ps)
ep-DCO	86.45	295.6
CDFF	28.71	121.0
SCDFF	12.03	85.08
MHLFF	11.10	75.04
SCCR	10.34	66.75
Proposed design	10.17	65.07

V. CONCLUSION

The different conventional explicit type flip flops such as explicit data close to output(ep-DCO),conditional discharge flip flop(CDFF),static conditional discharge flipflop(SCDFF),modified hybrid latch flip flop(MHLFF) and the implicit type flip flop named single ended conditional energy recovery(SCCR) are analysed.The power and delay calculation of conventional pulse triggered flip flops are done. The proposed low power flip flop using signal feed through scheme is deigned. The power and delay calculation of the proposed design is carried out. A low power counter is designed using the proposed flip flop design.

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