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Implementation of Low Power TPG using LFSR and single input changing generator (SICG) for BIST Application

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Abstract: A novel test pattern generator which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. A new low power test pattern generator using linear feedback shift register (LFSR), called LP-TPG, and is presented to reduce the average power and peak power of the circuit by reducing the switching activities during test. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive–ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. The proposed scheme is evaluated by using, a synchronous pipelined 4x4 and 8x8 Braun array multipliers. The system-on chip (SoC) approach is adopted for implementation on Xilinx Field Programmable Gate Arrays (FPGAs). From the implementation results, it is verified that the testing power for the proposed method is reduced by a significant percentage.

Keywords: BIST, Test Pattern Generator, LFSR, FPGA.

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits. Complex VLSI testing problems, such as built-in self-test (BIST) technique has been extensively studied and widely used now days. This approach introduces the embedded test structure into the circuit under test (CUT) to make testing easier and better. As we know built-in self-test (BIST), the test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware, minimizing hardware overhead which is a major concern of BIST implementation. Unlike stored pattern BIST, which requires high hardware overhead due to memory devices required to store pre-computed test patterns, pseudorandom BIST, where as test patterns are generated by Pseudorandom pattern generators such as linear feedback shift registers (LFSRs) and cellular automata (CA), requires very little hardware overhead. The linear feedback shift register (LFSR) is commonly used as a test pattern generator (TPG) in low overhead built-in self-test (BIST). This is due to the fact that an LFSR can be built with little area overhead and used not only as a TPG, which provides high fault coverage for a large class of circuits, but also as an output response analyzer. A significant correlation exists between consecutive vectors applied to a circuit during its normal operation. This fact is what has motivated several architectural concepts, such as cache memories, and is central to their effectiveness. This is also true for the high-speed circuits that process digital audio and video signals the inputs to most of whose modules change relatively slowly over time to time. In contrast, the consecutive vectors of a sequence generated by an LFSR are having low correlation. Since the correlation between consecutive vectors applied to a circuit during BIST is significantly lower, the switching activity in the circuit can be significantly higher during BIST than during its normal operation. Excessive switching activity during test can cause several problems. Foremost, since power dissipation in a CMOS circuit is proportional to weighted switching activity, a circuit under test (CUT) can be permanently damaged due to high temperature that is caused by excessive power dissipation if the switching activity in the circuit during test application is much higher than that during its normal operationfor a specific purpose and it is usually restricted by space, cost, storage and bandwidth, etc., so it must be made to measure on hardware and software to the utmost extent to improve efficiency and such results finally increase its real-time property.

In addition to this, the development of Intellectual Property (IP) cores for the FPGAs for a variety of standard functions including processors, enables a multimillion gate FPGA to be configured to contain all the components of a platform based FPGA. Development tools such as the Altera System-On-Programmable Chip (SOPC) builder enable the integration of IP cores and the user designed custom blocks with the Nios II soft-core processor. Soft-

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core processors are far more flexible than the hard-core processors and they can be enhanced with custom hardware to optimize them for specific application. Power dissipation is a challenging problem for today's System-on-Chips (SOCs) design and test.

In general, the power dissipation of a system in test mode is more than in normal mode. Four reasons are blamed for power increase during test.

- High switching activity due to nature of test patterns
- Parallel activation of internal cores during test
- Power consumed by extra design-for-test(DFT) circuitry
- Low correlation among test vectors

This extra average and peak power consumption can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product field and life time.

Thus special care must be taken to ensure that the power rating of circuits is not exceeded during test application. Different types of techniques are presented in the literature to control the power consumption.

These mainly includes algorithms for test scheduling with minimum power, techniques to reduce average and peak power, techniques for reducing power during scan testing and BIST(built-in-selftest) technique. Since off-chip communication between the FPGA and a processor is bound to be slower than onchip communication, in order to minimize the time required for adjustment of the parameters, the built in self test approach using design for testability technique is proposed for this case.

The rest of the paper is organized as follows. In section II, Previous works relevant to power reduction are discussed. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII, the implementation details and the results are presented. Section VIII summarizes the conclusion.

II. LITERATURE REVIEW

Krishnendu chakrabarty and Shivakumar swaminathan[2](Duke University, Durham), have presented built-in self testing of high-performance circuits using twisted-ring counters. They presented enhanced built-in self-test (BIST) architecture for high-performance circuits. This approach is especially suitable for embedding pre-computed test sets for core-based systems since it does not require a structural model of the circuit, either for fault simulation or for test generation. It utilizes a twisted-ring counter (TRC) for test-per-clock BIST and is appropriate for high-performance designs because it does not add any mapping logic to critical functional paths. Test patterns are generated on-chip by carefully reseeding the TRC. They showed that a small number of seeds are adequate for generating test sequences that embed complete test sets for the ISCAS benchmark circuits.

Mehrdad Nourani, Mohammad Tehranipoor[3] presented their research work on Low-Transition Test Pattern Generation for BIST-Based Applications. In their work; a low-transition test pattern generator, called the low transition linear feedback shift register (LT-LFSR), is proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions: 1) between consecutive patterns (fed to a combinational only circuit) and 2) between consecutive bits (sent to a scan chain in a sequential circuit).

LT-LFSR is independent of circuit under test and flexible to be used in both BIST and scan-based BIST architectures. Their proposed architecture increases the correlation among the patterns generated by LT-LFSR with negligible impact on test length. The experimental results for the ISCAS'85 and '89 benchmarks confirm up to 77 percent and 49 percent reduction in average and peak power, respectively.

Dilip kumar, B.Viswanathan[4] presented their research work on Implementation of BIST Test Generation Scheme based on Single and Programmable Twisted Ring Counters. Twisted-ring-counters (TRCs) have been used as built-in test pattern generators for high-performance circuits due to their small area overhead and simple control circuitry. When compared to other pattern generators TRC often requires long test time to achieve high fault coverage and large storage space to store required control data and TRC seeds. Programmable Twisted Ring Counter-based on-chip test generation scheme is to minimize both the required test time and test data volume. Programmable Twisted Ring Counter operates on test per clock method to reduce the test time.
To reduce the storage data for testing, seed and control vector determination process is used to achieve the less storage data in ROM.

P.Venkata Gopikumar, C.Ravishankar reddy[5] presented their work on Fault Detection by Using Random and Deterministic Test Pattern Techniques in a Mixed-Mode BIST Environment. In their work; A method for testing embedded core based system chips is to use a built-in-self-test (BIST). A mixed-mode built-in-self-test (BIST) brings two new techniques. They are partial pattern matching and multi control sequence. Partial pattern matching allows the reduction of the number of patterns used for detecting random-pattern-resistant faults without using the fault

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simulation. A multi control sequence is used to guide the linear feedback shift register (LFSR) to generate these patterns at application time. The main advantages of this method are reduction of the test data volume; require less time to test the application and its reusability for logic cores on a system-on-chip (SOC).

K.Veena Madhavi, M.Nirmala[6] presented their work on Efficient Weighted Pattern Generation Technique with Low Hardware Overhead. In their work Weighted pseudorandom built-in self test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power.

In this work an accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favourably with respect to the required hardware.

K. Nivitha, Anita Titus [7] presented their work on A BIST Circuit for Fault Detection Using Recursive Pseudo-Exhaustive Two Pattern Generator. A Built-in self-test (BIST) technique based on pseudo-exhaustive testing is proposed in this work. Two pattern test generator is used to provide high fault coverage. Testing for delay and sequential faults requires two-pattern tests. In two-pattern testing all possible combinations of the test vectors are applied to the circuit under test. In this paper a pseudo exhaustive two-pattern generator with fewer hardware that generates two-pattern (7, k)-adjacent bit pseudo exhaustive tests for any k<7 is used. Two circuits like Wallace tree multiplier and cryptographic circuit based on RSA algorithm are tested in parallel. The main advantage of this BIST is that the circuits have different cone sizes are tested at a time. This increases the speed of the BIST.

III. ANALYSIS OF POWER FOR TESTING

Power in electronic devices is defined as the conversion of electrical energy of power supply to heat. Equation (1) represents the power dissipation in electric circuits.

$$P=V.I \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

Where:
V = Voltage (Joules/Coulomb or Volts)
I = Current (Coulombs/Sec or Amperes)
P = Power (Joules/Sec or Watts)

CMOS technology is the best choice for low-power designs because of its insignificant static power dissipation. However, simply selecting CMOS technology should not be considered as the only method for reducing power in ASIC/SOC devices. Since most of today's designs are based on CMOS technology, the first step toward power reduction is to understand the sources of power dissipation in such devices. Power consumption sources in digital CMOS circuits are divided into three main categories:

- Static power dissipation
- short-circuit power dissipation
- Dynamic power dissipation

Equation (2) illustrates the relationship between these three parameters.

$$P_{Average}=P_{Static}+P_{Dynamic}+P_{Short\ circuit} \quad \ldots\ldots \quad (2)$$

CMOS devices have very low-static power dissipation and most of the energy in them is used to charge and discharge load capacitances. By comparison, the short circuit and static powers are usually of smaller magnitude than the dynamic power, and they can be ignored. Therefore, dynamic power is the principal source of power dissipation in CMOS devices. The following sections explain each of these power dissipation sources in detail.

1. Static Power Dissipation

Static power dissipation occurs when the logic-gate output is stable; thus it is frequency independent.

$$P_{Static}=V_{DD}.\ I_{leakage} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

2. Short-Circuit Power Dissipation

Short-circuit power dissipation occurs when current flows from power supply (VDD) to ground (GND) during switching. The value of short-circuit dissipation depends on the amount of short- circuit current flowing to GND.

$$P_{Short\ Circuit}=V_{DD}.\ I_{Short\ Circuit} \quad \ldots\ldots\ldots\ldots\ldots \quad (4)$$

3. Dynamic Power Dissipation

Dynamic power is the dominant source of power dissipation in CMOS devices and accounts for approximately 90 percent of overall CMOS power consumption. It occurs during the switching of logic gates, and as a result, this type of power dissipation is frequency dependent. Dynamic power is therefore the average power required to perform all the switching events across the circuit.

$$P_{Dynamic}=\beta.\ C.\ V_{DD}^{2}.\ F \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

Where:
β = Switching Activity per node
C = Switched Capacitance
F = Frequency (switching events per second)
V_{DD} = Supply Voltage

Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

$$E_i=\frac{1}{2}Vdd^{2}C_OF_iS_i \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (6)$$

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Where Vdd is the supply voltage, C_0 is the load capacitance. The product of F_i and S_i is called weighted switching activity of internal circuit node i.
The average power consumption of internal circuit node I can be given by,

$$P_i=\frac{1}{2}Vdd^2C_OF_iS_i\,f \quad \text{.....} \quad (7)$$

f is the clock frequency. The summary of P_i of all the nodes is named as average power consumption. It can be observed from (6) and (7) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.

A. BIST Approach:

Built-In Self-Test (BIST) has emerged as a promising solution to the VLSI testing problems. BIST is a DFT methodology aimed at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as improved testability, at-speed testing and reduced need for automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates test patterns and a multiple input shift register MISR) compacts test responses. Test vectors applied to a circuit under test at nominal operating frequency may have more average and/or peak power dissipation than those in normal mode. The reason is that the random nature of patterns reduces the correlation between the pseudorandom patterns generated by LFSR compared to normal functional vectors. It results in more switching and power dissipation in test mode.

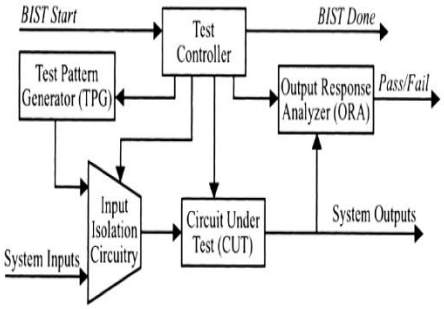

Figure 1: BIST basic block diagram

BIST is a design for testability (DFT) technique in which testing is carried out using built–in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR).A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer.

A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register[LFSR].The circuit introduces more switching activities in the circuit under test (CUT)during test than that during normal operation. It causes excessive power dissipation and results in delay penalty into the design.

B. Classification of test strategies:

1. Weighted Pseudorandom Testing: In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.

2. Pseudo exhaustive Testing: Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.

3. Pseudorandom Testing: Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.

4. Exhaustive Testing: Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT).It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.

5. Stored Patterns: Stored-pattern approach tracks the pregenerated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

IV. DESIGN OF MULTIPLIER

Multipliers are widely used in DSP operations such as convolution for filtering, correlation and filter banks for multi rate signal processing. Without multipliers, no computations can be done in DSP applications. Multipliers are one the most important component of many systems. So we always need to find a better solution in case of multipliers. Our multipliers should always consume less power and cover less power. For that reason, multipliers are chosen for testing in our proposed design.

Braun array multiplier is selected among various multipliers as it follows simple conventional method. The

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Braun array is the simplest parallel multiplier. All the partial products are computed in parallel, and then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder Also, pipelined Braun array multiplier is selected as it is faster in speed than non-pipelined multiplier. To avoid carry propagation delay at every stage, the carry bits are propagated to the next stage. Finally at the last stage, ripple carry adder is used to get the product term of P_4 to P_7.

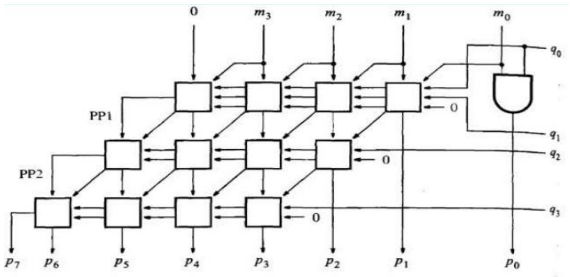

Figure 2: Braun array multiplier

V. PROPOSED METHOD

Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns. In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter; gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence.

The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

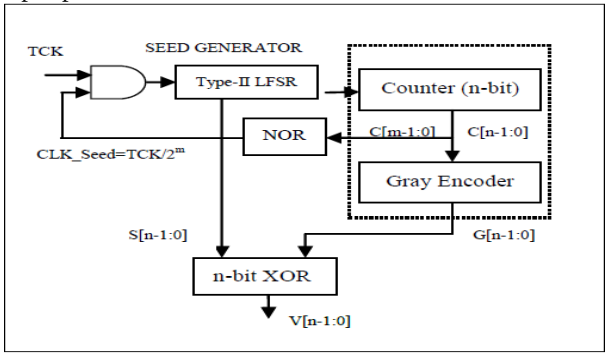

Figure 3. Proposed design of Low Power TPG.

According to the design the proposed structure of LP-TPG C [n-1:0] is the counter output and G[n-1:0] is the gray encoder output. The counter and SG are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates 2n continuous binary data periodically. The output of NOR operation of C [m-1:0] will be the clock control signal of SG where m<=n. It can be found that SG will generate the next seed only when C [m-1:0] are all 0 and NOR output changes to1. The period of the single input changing sequences will be 2m.Gray encoder in Fig. 1 is used to encode the counters output C[n-1:0] so that two successive values of its output G[n-1:0] will differ in only one bit. Gray encoder can be implemented by following logic.

G [0] = C [0] XOR C [1]
G [1] = C [1] XOR C [2]
G [2] = C [2] XOR C [3]
…….
G [n-2] = C [n-2] XOR C [n-1]
G [n-1] = C [n-1]

The seed generating circuit SG is a modified LFSR which is the combination of a Type-II LFSR and several XOR gates. The theory in [8] stated that the conventional LFSR's outputs can't be taken as the seed directly, because some seeds may share the same vectors. So the seed generator circuit should make sure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. The final test patterns are implemented as following logic.

V [0] = S [0] XOR G [0]
V [1] = S [1] XOR G [1]
V [2] = S [2] XOR G [2]
…
V [n-1] = S [n-1] XOR G [n-1]

The Seed Generator's clock will be TCK/2m due to the control signal. As SICG"s cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too. Fig 4 is the circuit structure of single input changing generator (SICG), which consists of an n-bit counter and a Gray code encoder.

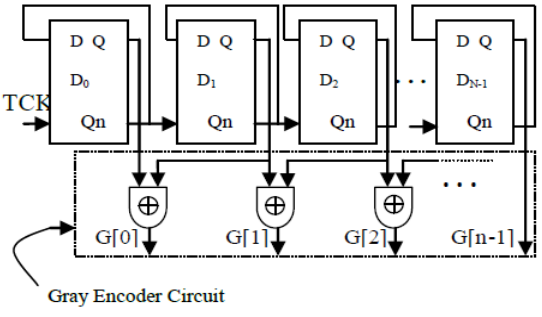

Figure 4: Circuit structure of single input changing generator (SICG).

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The n-bit counter consists of n D flip-flops and the gray encoder consists of n-1 exclusive-OR gates. So the hardware overhead can be controlled under reasonable scope and the power consumption can be greatly reduced while the fault coverage is guaranteed. It is applicable for large scale circuits especially for SoC.

VIII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

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