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Five Level Output Generation for Hybrid Neutral Point Clamped Inverter using Sampled Amplitude Space Vector PWM

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Abstract: A space vector pulse width modulation signal generation for the five level hybrids neutral point clamped inverter using only the sampled amplitude of the reference phase voltage is proposed in this paper. This Pulse widthmodulation scheme generation in the inverter leg switching times, from the sampled reference phase voltage amplitude and centers the switching times for the middle vectors in a sampling interval. This PWM technique does not require any sector identification and it reduces the computational time compared with the conventional space vector pulse width modulation technique. In this technique the centering of the middle inverter switching of the SVPWM is achieved by the addition of the offset time signal to the inverter gating signal, derived from the sampled amplitude of the reference phase voltage.

Keywords: Neutral Point clamped multilevel inverter, SPWM, Sampled Amplitude Space Vector PWM Signal Generation.

I. INTRODUCTION

Due to the advancement in the semiconductor devices, medium voltage adjustable speed drives are mainly used in the industrial applications to conserve the electrical energy, increase the productivity and to improve the product quality. They are mainly used for pipeline pumps in the petrochemical industry, fan in the cement industry, pumps in the water pumping station, traction application in the transportation industry, steel rolling mills in the metal industry etc. Market research show that around 85% of the total installed drives are for pumps, fans, compressors and conveyors where the drive system might not require high dynamic performance.

Induction motor is also being used extensively in application requiring fast and accurate control of speed and torque. In most industrial application three phase induction motors are used. The other reason for using the induction motor in most of the industrial application is that, they are cheapest andrugged.

For the smooth working of the induction motor the inverters are used. The inverters are mainly classified into voltage source inverters and the current source inverters. Depending upon thelevel of output voltage both of them are again classified into two level inverters and the multilevel inverters. When the level is increased the harmonics in the output voltage will bereduced.

The multilevel voltage source inverter is again classified into three. They are Neutral Point Clamped inverter (NPC), flying capacitor clamped inverter and the cascaded H-bridge inverter. From these for the application of drive mostly select the neutral point clamped inverter and the cascaded H-bridge inverter. One aspect of cascaded multilevel inverter apart from the three level NPC inverter is to utilize small inverter bridgeswith relatively low voltage to synthesize and reach high voltage. Thus it is more suitable for high voltage, high power application [1]. But in most of the causes they use the cascadedH-bridge inverter. But the main drawback of H-bridge inverter is that the need of excessive number of transformer windings. To eliminate this drawback, a hybrid inverter of cascaded and NPC structures, the cascaded neutral point clamped inverter was introduced [2], [3]. For the inverters, different types of modulation strategies are used. From this the most popularly used are carrier based pulse width modulation (PWM)[4], [5] space vector modulation (SVM)[6] and the step modulation.

Most carrier based modulation schemes for the neutral point clamped inverter derive from carrier disposition strategy. According to the arrangement of carrier they are classified into Phase Opposition Disposition (POD), Alternative POD, and Phase Disposition (PD). From this the most accepted one is PD because there will be the lowest line to line harmonics voltage distortion at the output. When the number of carriers increases, it is difficult during the implementation of hardware. So the number of carriers will be reduced to reduce the hardware burden. So when we use a single carrier concept, it produces the required SPWM signals by chopping the reference signals into single carrier range according to the magnitude.

The nominal SPWM technique are more flexible and easy to implement. But the maximum peak of the fundamental component in the output voltage is limited to 50% of the dc link voltage. In case of SVPWM scheme, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time duration in a sampling interval. The SPWM scheme gives a more fundamental voltage and better harmonics performance compare to the SPWM scheme. But the conventional

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SVPWM requires the sector identification and the look up tables to determining the timing for various switching vectors of the inverter, in all sectors. So the implementation of conventional PWM is verycomplicated. So a new scheme is proposed for PWM signal generation for the multilevel inverter similar to the SVPWM, for the entire range of modulation indices including the over modulation [7]. The PWM switching times for the inverter leg are directly derived from the sampled amplitude of the reference phase voltages.

This paper proposes a new modulation scheme for the hybrid neutral point clamped inverter. In this paper there will be a five level hybrid neutral point clamped inverter. The modulated pulse will be produced by using the sampled amplitude of reference phase voltages. In this method there will be a single carrier and the sine wave as the modulating signal.

II. HYBRID NPC INVERTER

In the industrial field the three phase induction motors are mainly used and inverters are needed for its driving. The balancing of capacitors is difficult when the neutral point clamped inverters are used. So in each phase there will be a hybrid inverter which is the combination of NPC inverter and the cascaded H-bridge inverter is used. One module of hybrid neutral point clamped inverter is given in Fig. 1

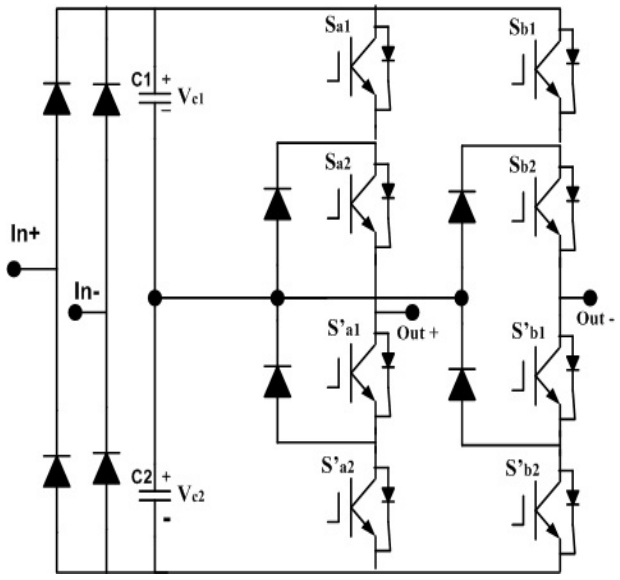

Fig.1 NPC module

It consists of eight switch in eachphase. By using this it produces the five level output voltage. The eight switches are named as S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{a1}', S_{a2}', S_{b1}', and S_{b2}'. The eight isolated switching signals are sending to the switch through the eight isolated drive circuit. The high level of switching signal makes the switch on and the low level of switching signals make the switch off.

The Table I show the output voltages and their switching states, along with which capacitor is used when applicable. During the operation it uses two capacitors. Both of them are balanced during the operations. That means the average output voltage across the capacitors are same ie.,$V_{C1} = V_{C2}$. By the utilization of these capacitors five levels of voltages are produced at the output.

TABLE 1 SWITCHING SEQUANCE, CAPACITOR USED, OUTPUT VOLTAGE

S_{a1}	S_{a2}	S_{b1}	S_{b2}	S'_{a1}	S'_{a2}	S'_{b1}	S'_{b2}	Capacitor used	Output Voltage
0	0	0	0	0	0	0	0	None	Protective
0	1	0	1	1	0	1	0	None	0
0	1	0	0	1	0	1	1	C_2	$+V_{c2}$
1	1	0	0	0	0	1	1	C_1,C_2	$+V_{c2}+V_{c1}$
1	1	0	1	0	0	1	0	C_1	$+V_{c1}$
0	1	1	1	1	0	0	0	C_1	$-V_{c1}$
0	0	1	1	1	1	0	0	C_1,C_2	$-V_{c1}-V_{c2}$
0	0	0	1	1	1	1	0	C_2	$-V_{c2}$

III.PWM SIGNAL GENERATION

A. Sine PWM

In the sine PWM technique the generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with high frequency triangular carrier. Depending on weather the signal is greater or smaller than the carrier waveform the pulse will be produced. Over the period the period of one triangular wave, the average voltage applied to the load is proportional to the amplitude of the modulating signal at that period.

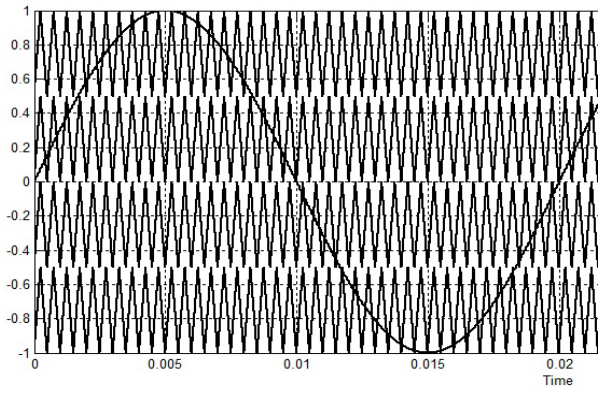

Fig.2 Multicarrier sine PWM

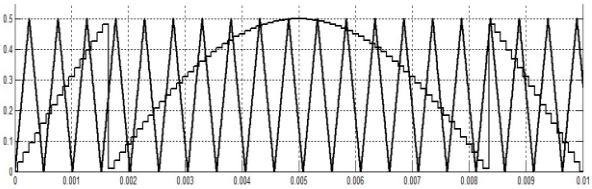

Fig.3 Single Carrier Sine PWM

For a five level inverter normally it requires four carriers. The Fig. 2 shows the multiple carrier sine PWM technique for the five level inverter. As the level of inverter increases the carrier requirement increases, which is quite difficult for the hardware implementation. The introduction of single carrier concept overcomes the problem. In the single carrier concept, it chopped the reference signal into the single carrier range according to the magnitude. The Fig. 3 shows the single carrier based sine PWM.

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B. Space vector PWM signal generation using the sampled amplitude of reference phase voltage

To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, a common mode voltage $V_{offset1}$ is added to the reference phase voltage [18], where the magnitude of offset voltage is given by,

$$V_{offset1} = -(V_{max} + V_{min})/2 \quad (1)$$

In (1) $V_{max}$is the maximum magnitude of the three sampled reference phase voltage and the minimum magnitude of the three sampled reference phase voltage in a sampling interval is represented by V_{min}This equation is based on the fact that during the sampling time period Ts, the reference phase voltage which has the lowest magnitude crosses the carriersfirst and the reference phase voltage which has the highest magnitude crosses the carriers last. But the offset voltage computation base on equation (1) is not sufficient to centering middle inverter switching vectors of multilevel inverter switchingvectors of multilevel inverter in the sampling period Ts. So another technique based on the sampled amplitude of thereference phase voltage will be used. By using this techniquethe time instant at which the three reference phase crossesthe triangular carrier is determined. Then by using this timeinstant the offset voltage to be added to the reference phasevoltage is calculated. The steps involved for the calculationsare

1) Calculate the$V_{offset1}$.

2) The modified reference voltage is

$$V^*_{Xn} = V_{Xn} + V_{offset1} \quad (2)$$

X= A,B,C

Where the V_{AN}, V_{BN} and $V_{CN}$are the sampled amplitude of the three reference phase voltage.

3)CalculateT_{across}, T_{bcross}andT_{ccross}. When the number of levels of multilevel level inverter is odd then,

$$T_{across} = T^*_{as} + ((I_a - (n-1)/2) * T_s) \quad (3)$$
$$T_{bcross} = T^*_{bs} + ((I_b - (n-1)/2) * T_s) \quad (4)$$
$$T_{ccross} = T^*_{cs} + ((I_c - (n-1)/2) * T_s) \quad (5)$$

T_{across}, T_{bcross}andT_{ccross} denotes the time durationat which the three phase voltage a, b and c crosses the triangular carrier. A carrier index I is defined to designate the carrier region in which the reference phase voltage lie during the sampling interval.

4) Determine

$$T_{first\ cross} = \min(T_{x\ cross}) \quad (6)$$
$$T_{second\ cross} = \mathrm{mid}(T_{x\ cross}) \quad (7)$$
$$T_{third\ cross} = \mathrm{mid}(T_{x\ cross}) \quad (8)$$

where x=a, b, c.

5) Determine

$$T_{middle} = T_{third\ cross} - T_{first\ cross} \quad (9)$$

6) Determine the time duration of the start and end vector.

$$T_0 = T_s - T_{middle} \quad (10)$$

7) Calculate the time duration of the start vector

$$T_0/2 = T_{first\ cross} + T_{offset2} \quad (11)$$

Therefore

$$T_{offset2} = T_0/2 - T_{first\ cross} \quad (12)$$

8) The value of $T_{offset2}$is added to T_{across}, T_{bcross}andT_{ccross}.

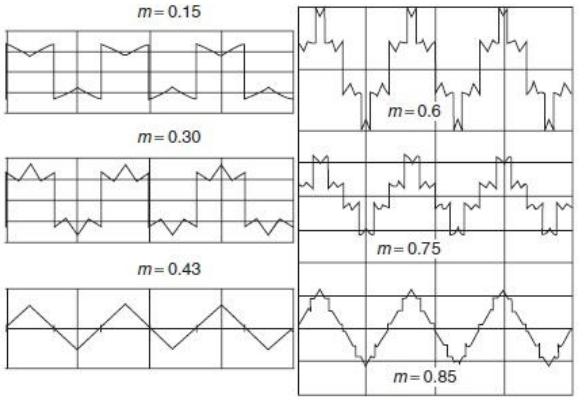

Fig. 4 profile of $T_{offset1}$+$T_{offset2}$for different modulation indices

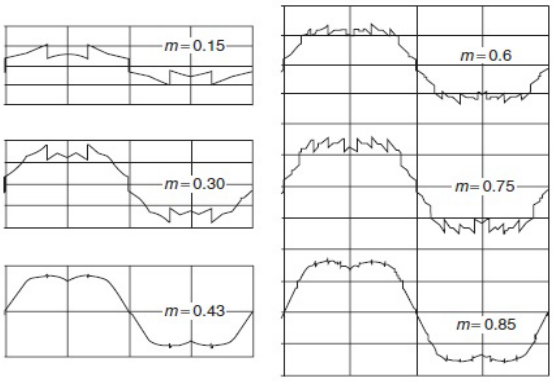

Fig. 5 profile of T^*_{as}+$T_{offset2}$ for different modulation indices

C. Pulse Decoding

The pulse that produced by SPWM will be decoded into different levels to produce the five level output voltage. For this three binary variables a, b, and c are used. For a five level inverter, when a=0 represents the positive half cycle of the reference whereas a=1 represents the negative half cycle of the reference. When b=0 represents the positive slope of the reference whereas b=1 represents the negative slope of the reference and c locate the position of reference with respect to carrier. The utilization of capacitor C_1 and C_2 will exchange in the same module if the variable b is reversed.

IV. SIMULATION RESULT

The simulation of the hybrid inverter with a new PWM topology is done in MATLAB R2011a. The PWM topology used here is the space vector PWM signal generation using only the sampled amplitude of the reference phase voltage. The inverter input is 340 V dc. The overall model of simulation is given in Fig. 6.

In the first sub system three phase voltages is generated in the time axis which is shown in Fig. 7.

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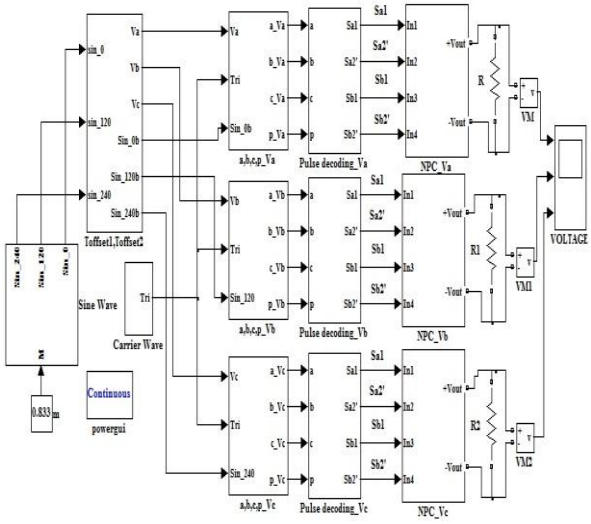

Fig. 6 Simulation model

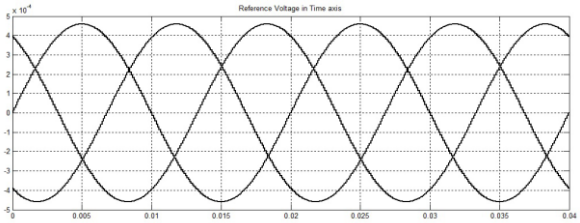

Fig. 7 Three phase reference voltage in time axis

In the subsystem2$T_{offset1}$and $T_{offset2}$is generated. $T^*_{as}+T_{offset2}$for the different modulation index can be shown in Fig. 8 and Fig. 9. That two offset values are added with reference phase voltage. Then the output voltages V_a, V_b and V_c, are produced. The modified reference phase voltage is shown in Fig 10, Fig. 11, and Fig. 12.

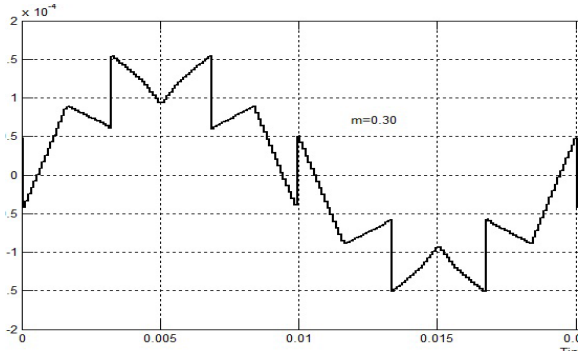

Fig. 8: $T^*_{as}+T_{offset2}$for the modulation index m=0.30 the next subsystem the reference voltage is compared with the triangular carrier of 2:5 kHz. The pulse produced by the comparing of triangular and reference phase voltage is decoded by using the three binary variables, a, b and c.

For afive level inverter when a=0 represents the positive half cycle of the reference and a=1 represents the negative half cycle of the reference. When b=0 represents the positive slope of the reference and b=1 represents the negative slope of the reference and c locate the position of reference with respectto carrier. The decoding variables are shown in Fig.13.

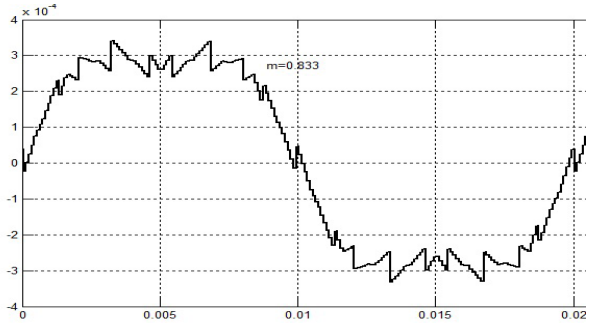

Fig. 9 $T^*_{as}+T_{offset2}$ for the modulation index m=0.85

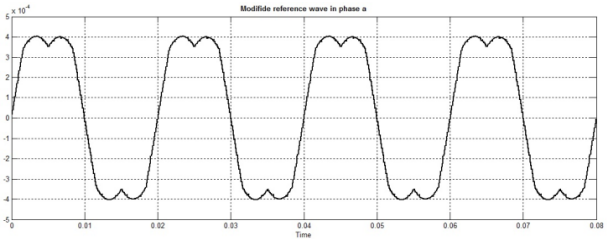

Fig. 10 Modified reference phase voltage V_a

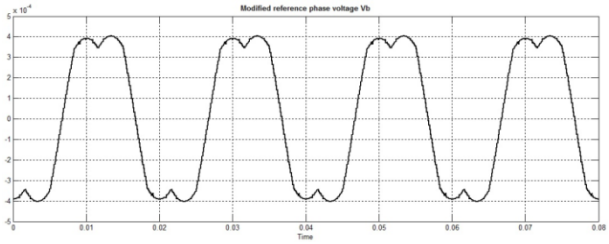

Fig. 11 Modified reference phase voltage V_b

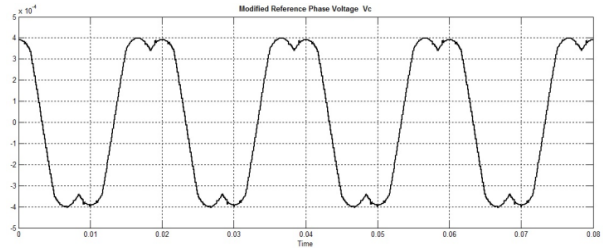

Fig. 12 Modified reference phase voltage V_c

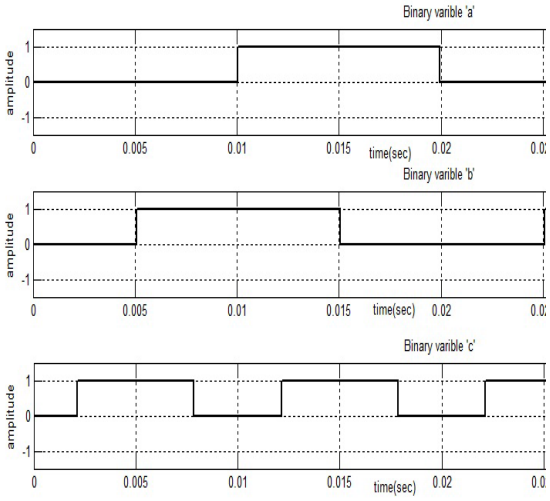

Fig. 13 Decoding variables a, b and c

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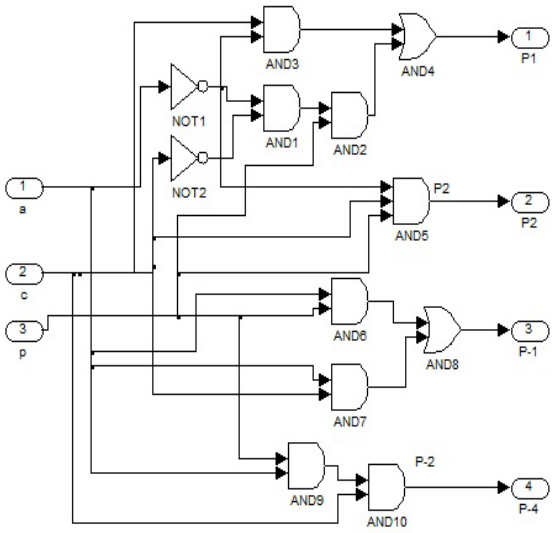

Fig. 14 Decoding circuit for four pulses

The variable 'p' represent the pulses that produced during the PWM. The pulse 'p' will be decoded into four pulses in subsystem6, subsystem7 and subsystem8. This decoding of pulse into four pulses is given in Fig. 14. The four pulses are given in Fig. 15.

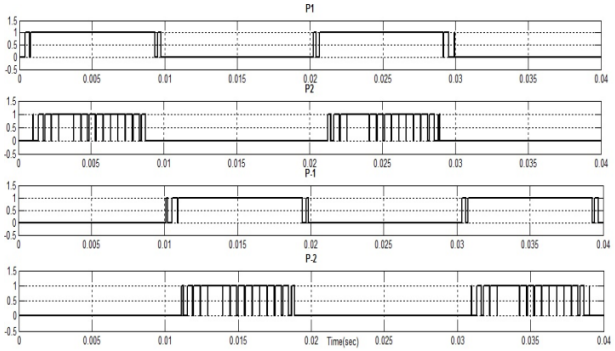

Fig. 15 Four pulse

This pulses will again decoded into different pulses for each switches in the differentphases. The switching pulses will be shown in Fig.16.

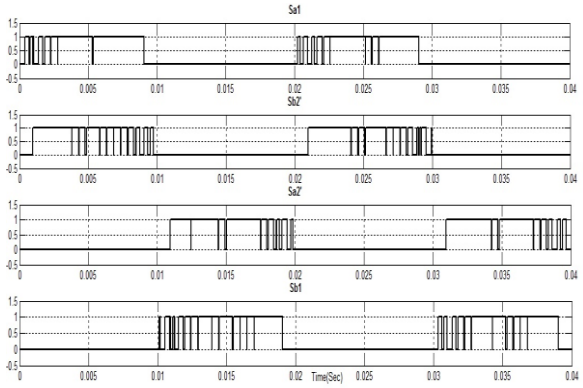

Fig. 16 switching pulse

The output waveform produced by hybrid inverter is given in Fig. 17.

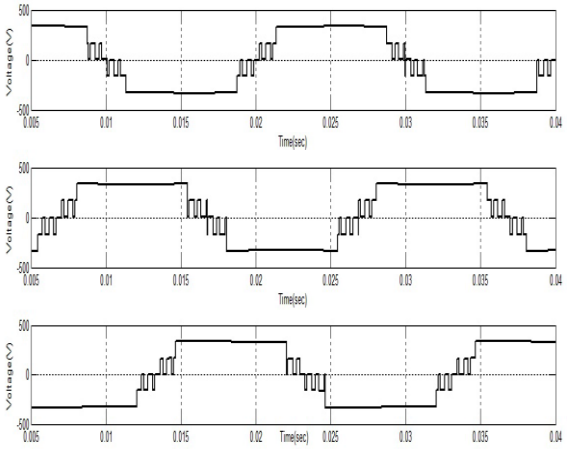

Fig. 17 Five level phase voltage of the hybrid inverter

V. CONCLUSION

This paper presents an effective modulation technique for the hybrid NPC inverter. This module of hybrid NPC inverter can produce the five levels of output by using the two capacitors. To increases level of output, cascaded this hybrid NPC inverter in each phase. In this paper a voltage modulation scheme of the SVPWM has been presented for the hybrid NPC inverter. The centering of the middle inverter switching vectors of the SVPWM is achieved by the addition of anoffset time signal to the inverter gating signal, derived from thesampled amplitudes of thereference phase voltages. The PWMtechnique presented in this paper does not need any sector identification. So the complicated calculation and the look-up tables can be avoided by usingthis method. This reduces the computational time required to determine the switching times for the inverter leg, making this technique suitable for the real time implementation.

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