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Analysis and Design of a New Modified Double-Tail Comparator for High Speed ADC Applications: A Review

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Abstract*: :* Analog-to-digital converters (ADCs) are key design blocks and are currently adopted in many application fields to improve digital systems, which achieve superior performances with respect to analog solutions. Application such as wireless communication and digital audio and video have created the need for cost effective data converters that will achieve higher speed and resolution. Comparator is one of the main building blocks in most analog-to-digital converters. Many high speed analog to-digital converters, such as flash ADCs, require high-speed, low power comparators with small chip area. In low power, area efficient, and high speed analog-to-digital converters we need dynamic regenerative comparators to increase speed and power efficiency. In this paper, a new dynamic comparator is proposed, where the circuit of a low voltage low power double tail comparator is modified for area efficient and double edge triggered operation. This paper provides a comprehensive review about a variety of comparator designs - in terms of performance, power and delay using Cadence Virtuoso CMOS 180-nm technology.

Keywords: ADC (Analog to Digital Converter), CMOS (Complementary Metal Oxide Semiconductor), dynamic comparators, Cadence Virtuoso**.**

I. INTRODUCTION

In electronics, Operational amplifier (Op-amp) is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Op-amp. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, data transmission, and others. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input analog signal with a reference analog signal and outputs a binary signal based on comparison.

These days dynamic comparator are used for reducing power dissipation and increase the conversion rate of analog to digital. Back-to-back inverters in dynamic comparators provide positive feedback. By this mechanism we can convert a smaller voltage difference in full scale digital level output.Fig.1. shows the schematic symbol of the comparator and Fig.2 shows its ideal transfer characteristics. V_P is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and V_n is the reference voltage (constant DC voltage) applied to the negative terminal of comparator.

Now if V_p , the input of the comparator is at a greater potential than the V_n, the reference voltage, then the output of the comparator is a logic 1, where as if the V_p is at a potential less than the V_n , the output of the comparator is at logic 0.

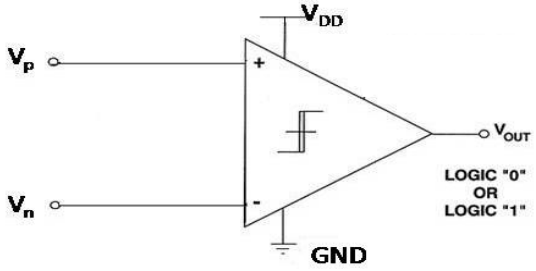

Fig.1. Schematic symbol of comparator

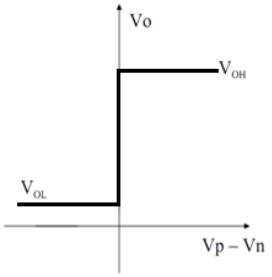

Fig 2. Ideal voltage transfer characteristic of comparator

If $V_p > V_n$, then V_o= logic 1.
If $V_p < V_n$, then V_o= logic 0.

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Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region of the analog signal. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into several comparator architectures. They are discussed in as follows.

A. COMPARATOR ARCHITECTURES

Open loop comparator Open-loop, comparators are an operational amplifier without frequency compensation in comparator design to obtain the largest possible bandwidth and good frequency response, hence improving its time response. Since linearity of the design and the precise gain are of no interest in comparator design, no-compensation does not pose a big problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many designing applications. The gain-bandwidth product of cascaded of open-loop comparator usually larger than a single-stage amplifier with the same gain. The implementation design costs more area and large power consumption, and cascading does not give any practical advantages for different types of applications.

Regenerative comparator: The second architecture of comparator is Regenerative comparators (latches) use positive feedback to accomplish the comparison of two different analog signals. In the Fig. 3 shows basic NMOS latch and PMOS latch type. Latches have a faster switching speed and the propagation delay.

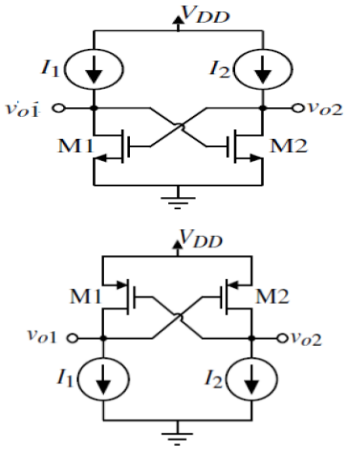

Fig 3. NMOS and PMOS Latch

High speed comparator: High speed comparator consists of regenerative comparator as well as open loop comparator. It mainly consists of three building blocks of comparator, Input stage, a flip-flop and S-R latch. It uses a preamplifier to build up the input change to a sufficiently large value of signal and then applying it to the 2nd stage latch. This architecture combines the best aspects of comparator with a negative exponential rise due to preamplifier stage at beginning and positive exponential rise due to latch stage. The main advantages of high speed comparator have a lower propagation delay and faster response time.

Dynamic Latch comparator: Today's most important comparator design technique is dynamic latch. Dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A dynamic latch is shown in Fig. 4.This latch circuit is driven by a clock. During one phase of the clock (clk =1) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk =0), the transmission gate opens and the inverter's output is determined by the node. The Setup and hold times of comparator is determined by the transmission gate must be taken in consideration in order to ensure proper operation of the latch i.e. adequate level of voltage is stored on the gate capacitance of the latch.

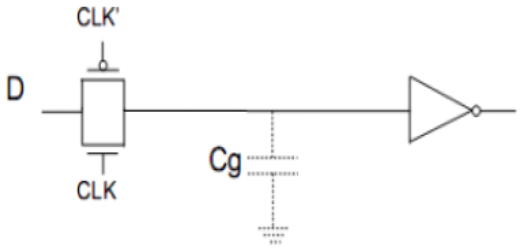

Fig 4. Dynamic latch

II. LITERATURE SURVEY

Literature survey is an important part of the project. It enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

Sougata Ghosh, Samraat Sharma presented a paper entitled as "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator",[1]. In this, investigation resulted in a novel dynamic latched comparator which has lower offset voltage and higher load drivability than the conventional dynamic latched comparators.

Wazir Singh et. al, presented CMOS comparators using preamplifier, suitable for high-speed analog-to-digital converters with High-Speed and Low Offset. The designs are mainly optimized for the low propagation time, minimal input resolution and minimal circuit area. Two comparator topologies, namely, double-clock preamplifier based comparator and single-clock preamplifier based comparator have been analyzed and designed. The topologies using preamplifier completely removes the offset that is present in the input of the latched comparator. Nearly 18 mV offset voltage achieved with the structures making them suitable for flash-type and pipeline data conversion applications [2].

Senthil Sivakumar M & Banupriya M designed pre-amplifier based comparators for the Flash ADC design and presented a paper entitled as "High Speed Low Power Flash ADC Design" [3] . In this, pre-amplifier based comparators have been used for ADC architectures such as

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flash and pipeline. The main drawback is the more offset voltage, large static power consumption.

The paper entitled as "**Analysis & Design of Low Power CMOS Comparator at 90nm Technology"**[4], presented by **Shruti Hathwalia.** In this dynamic latched comparators are used. They provide high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. But Dynamic latch comparators require sufficiently high supply voltage for a proper delay time.

Michel Rouger,Pierre Lutz et.al designed Low-Power Auto-zeroed High- Speed latch Comparator. The offset compensated comparator architecture used in this Work. The comparator uses both input offset storage and output offset storage. This allows eliminating the offset voltages of both the stages using only one-capacitor pairs and offset sampling phase [5].

Nikoozadeh et.al, gives the idea about how to analyze the effect of load capacitor and how minimize the mismatch on the offset of a regenerative latch comparator. The two analytical models are presented by author and compared with HSpice simulations. The simulation results indicate that in a typical 0.18-µm CMOS latch, a capacitive imbalance of only 1 fF can lead to offsets of several tens of mV. [6].

The structure of double-tail dynamic comparator first proposed in the paper **"A double-tail latch-type voltage sense amplifier with 18ps Setup + Hold time",**[7].A double-tail sense amplifier is presented here, which uses one tail for the input stage and another for the latching stage. This topology has less stacking and can therefore operate at lower supply voltages.

Heung Jun Jeon et.al, presented a novel dynamic latched comparator that demonstrates various efficient parameter like, lower offset voltage and higher load drivability compared to conventional dynamic latched comparators. In this novel design of the comparator circuit with two additional inverters inserted between the input and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented. The overall simulation results are better than the conventional double-tail dynamic latched comparator at approximately the same area and power consumption [8].

Yong-Bin Kim and Heungjun Jeon et.al, presented a paper in which A novel dynamic latched comparator with offset voltage compensation technique is discussed. The proposed comparator of offset compensation technique uses one phase clock signal for its operation and can drive a larger capacitive load with complementary version of the regenerative output latch stages [9].

Shaik Mastan Vali, Pyla Rajesh et.al, designed a comparator with low-offset voltage Fully Dynamic Latched Comparator with positive feedback for High-Speed and low-power ADCs application. The comparator used positive feedback mechanism with one pair of back-to-back cross coupled inverters in order to convert a small input-voltage difference to a full-scale digital level in a short time. So an input-referred latch offset voltage, resulting from static mismatches such as threshold voltage V_{th} and ß variations in the comparator regenerative latch, deteriorates the accuracy of such types of comparators [10].

Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman Soheil Ziabakhsh et. al, presented a novel design of CMOS dynamic latch comparator with dual input single output with the differential amplifier stage using charge sharing topology to achieve low power and high-speed operation. The designed dynamic latch comparator is required for high-speed analog-to-digital converters to get faster signal conversion and to reduce the power dissipation, which are immune to noise. The main challenge lies on the constant speed, which makes more critical; this faster speed has been gained by this proposed designed novel dynamic latch comparator with the combination of resistive dividing comparator and differential current sensing comparator. The topology of the proposed design is able to minimize the propagation delay and power consumption with the improved performances .Even, the different capacitor value and the transistor lengths produced the faster output, which is suitable for the successful operation of the ADC [11].

Samaneh and Reza Lotfi proposed a concept of analysis of double tail comparator in the paper entitled as **"Analysis and design of a low-voltage low-power double-tail comparator"**,[12], which included analysis of Conventional dynamic comparator, Conventional double tail comparator and Proposed double tail comparator and their analysis.

The paper entitled as **"Low Power High Performance Double-tail Comparator",[13],** by Umamaheswari.V.S ,Rajaramya.G. In this double tail comparator design includes VHDL coding and simulation using FPGA kit.

III. APPLICATIONS

1) N. Naga Sudha designed a High Speed and Low Power Dynamic Latch Comparator for PTL Circuit Applications**.** The designs of high-speed and low power dissipating clocked comparators are used for stack circuit applications. The comparator is attractive for the applications where both speed and power consumption **is** of the highest priority [14].

2) S. Yewale and R. Gamad presented an improved method for design of CMOS comparator based on a preamplifier latch circuit driven by a clock. This design is implemented in Sigma-delta Analog-to-Digital Converter (ADC). Thus, by considering factors of speed and resolution, preamplifier latch comparator are the choice for a high speed analog to digital converter. This type of latched comparator was also used for high speed and reduced power dissipation comparator performance [15].

3) S. Rahil Hussain, et.al, presented a High Speed and Low Power Dynamic Latched Comparator for Aircraft Application. These types of comparators are used in aircraft applications. The simulation results of three comparators show that the dynamic latched comparator

will occupy less active area and also having higher speed of operation and consumes less power. So by using the dynamic latched comparator in the application of aircraft is more efficient when compared to other comparator designs [16].

IV.CONCLUSION

This paper provides a brief analysis on different types of comparators and their performance analysis. In the proposed design a new modified double-tail comparator will be designed for ADC applications. The comparator will be designed using Cadence Virtuoso 6.1.1 Version, Analog Design Environment. Simulations will be carried out on different comparator to obtain the best results. Power and Delay analysis is major area of concern.

REFERENCES

[1]. Sougata Ghosh, Samraat Sharma, "A Novel Low-Power, Low-Offset and High- Speed CMOS Dynamic Latched Comparator", International Journal of Electronics and Computer Science Engineering, IEEE, 2010 ,Vol. 2, Number 1, pp. 411-426.

[2] Wazir Singh, "Study and Design of Comparator High Speed ADCs", Thapar University, Patiala, Department of Electronics and Communication Engineering,July- 2011.

[3]. Senthil Sivakumar M, Banupriya M, " High Speed Low Power Flash ADC Design" , International Journal of Scientific & Engineering Research, Vol. 3, Issue 5, May- 2012 , pp.290-295.

[4]. "Analysis & Design of Low Power CMOS Comparator at 90nm Technology", *Shruti Hathwalia et al Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 4(Version 1), April 2014, pp.289-292* .

[5] Yavuz De˘gerli, Nicolas Fourches, Michel Rouger, and Pierre Lutz. "Low-Power Autozeroed High- Speed Comparator" IEEE Transaction on Nuclear Science vol. 50 no.-5 oct.2003..

[6]. Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits Syst.II, vol. 53, no. 12, pp. 1398- 1402, Dec. 2006.

[7] Daniël Schinkel, Eisse Mensink, Eric Klumperink, Ed van Tuijl, Bram Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time", 2007 IEEE International Solid-State Circuits Conference. pp. 314–315.

[8]. Heung Jun Jeon, "Low-power high-speed low-offset fully dynamic CMOS latched comparator", Northeastern University, Department of and Computer Engineering, January 2010.

[9]. Yong-Bin Kim and Heungjun Jeon, "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator", IEEE press, 2010.

[10]. Shaik Mastan Vali1, Pyla Rajesh, "A 3GHz Low-offset Fully Dynamic Latched Comparator for High-Speed and Low-Power ADCs" International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 6, June 2013)

[11] Raja Mohd . Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz, and Labonnah Farzana Rahman," Design and Analysis of Low Power and High Speed Dynamic Latch Comparator in 0.18µm CMOS Process", *IJIEE Vol. 2, No. 6, pp*. 944-947, *November 2012*.

[12]. "Analysis and design of a low-voltage low-power double-tail comparator", proposed by Samaneh and Reza Lotfi, IEEE transactions on Very Large Scale Integration (VLSI) systems, vol. 22, no. 2, February 2014.

[13] Umamaheswari.V.S.,Rajaramya.G2,"Low Power High Performance Double-tail Comparator" , ISSN : 2277-1581,May 2014.

[14] N. Naga Sudha et. al, "High Speed and Low Power Dynamic Latched Comparator for PTL Circuit Applications"/International Journal of Computer Science and Information Technologies, (IJCSIT) Vol. 3 (1), pp-2982 – 2991, 2012.

[15] S.Yewale and R. Gamad, "Design of Low Power and High Speed CMOS Comparator for A/D Converter Application", *Wireless Engineering and Technology*, Vol.3, pp. 90-95, 2012.

[16] S. Rahil Hussain, N. Naga Sudha, V. Narasimha Nayak, Dr. Fazal Noor Basha, "High Speed and Low Power Dynamic Latched Comparator for Aircraft Application" / International Journal of Engineering Research and Applications (IJERA) Vol. 2, Issue 3, , pp.1301-1312, May-Jun 2012.

[17] Praveen J, MN Shanmukha Swamy, "Minimizing Test Power In VLSI architecture Using BIST Based Low-Transition Test Pattern Generation Technique", International Journal of Electronics and Communications Engineering and Technology, Vol – 5,pp -44-52, 2014.

[18] Praveen J, MN Shanmukha Swamy, "Low-Transition Test Pattern Generation For Minimizing Test Power In VLSI Circuits Using BIST Technique", International Journal Of Innovative Research In Electrical, Electronics, Instrumentation And Control Engineering, Vol – 2,pp -2029-2035, 2014.