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Improved Carrier Function and Optimal Structure for Stepped Wave Inverters

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Abstract: Multilevel inverters include an array of power semiconductor devices and capacitor voltage sources, the output of which cause voltages with stepped waveforms to have compact distortion. The term multilevel starts with the three-level inverter introduced by Nabae *et al*. The most attractive features of multilevel inverters include output voltages with extremely low distortion, lower dv/dt, input current with very low distortion, generate smaller common-mode (CM) voltage (thus reducing the stress in the motor bearings), lower switching frequency, etc. The main advantage of this topology is that it does not need additional diodes or capacitors for implementation. The operation of the flying capacitor multilevel inverter topology is based on the connection of capacitors, without using extra diodes. The most important advantage of this topology is that the number of switching combinations through which a same output voltage level can be achieved and hence allows a better distribution of the energy demanded from the capacitors. A new topology has to be proposed that provide higher number of level with optimum number of devices and dc voltage sources. A generalized structure has to be derived that brings easier implementation for desired output voltages for medium voltage applications. Also a new modulation technique is proposed which enhances the fundamental voltage and reduces the Total Harmonic Distortion (THD).

Keywords: Modified cascaded multi-level dc link inverter, Multi career PWM, 60^{o} PWM technique, THD

I. INTRODUCTION

In recent years industrial applications have begun to require higher power applications and medium voltage motor drives require medium voltage and megawatt power level as well. As a effect, a multilevel power converter structure has been introduced in 1975 as an alternative in high power and medium voltage applications through a series of power semiconductor switches with several low voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output and the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Subsequently, several multilevel converter topologies have been developed. The attractive features of a multilevel inverter are,

(i) Staircase waveform quality: Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

(ii) Common-mode (CM) voltage: Multilevel inverters produce smaller CM voltage; therefore, the stress in the motor bearings allied to a multilevel drive can be reduced.

(iii) Input current: Multilevel inverters can draw input current with low distortion.

(iv) Switching frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency based PWM. It would be eminent that lower switching frequency usually means lower switching loss and higher efficiency. Plentiful multilevel inverter topologies have engaged contemporary research on novel inverter topologies and unique modulation structures. Besides, three different foremost multilevel inverter structures have been reported in the literature: cascaded H-bridges inverter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Moreover, newer modulation techniques have been developed for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), which is simple an extension of two level modulation.

II. MODIFIED CASCADED MULTI-LEVEL DC-LINK INVERTER

Multilevel inverters uses small magnitudes of dc voltage sources typically from renewable energy sources, capacitor voltages to produce multistep waveform approximated to nearby sinusoidal voltage. One exact disadvantage is the greater number of power semiconductor switches required to produce more number of voltage steps.

Although lower voltage rated switches can be utilized in a multi-level inverter, each switch requires gate drive circuits. This is the basis for overall system to be complex and affluent. Moreover, this section focused on a new topology to reduce the number of power switches, gate driver circuits and power supplies.

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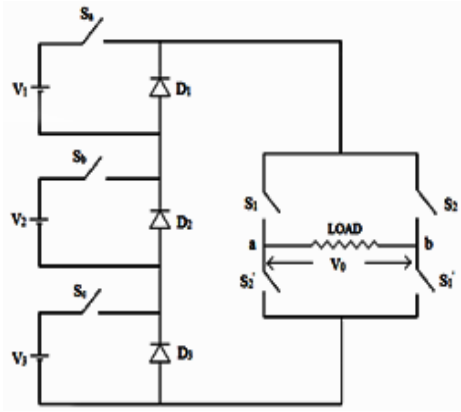

Fig.1. Generalized CMLDCLI

The proposed topology composed of several sub multilevel cells constituted by isolated voltage sources connected in series with power switch and a power diode in parallel as shown in Fig. 2.1. Each sub-multilevel cell is capable of producing three levels using only a dc source.

A. Modes of Operation

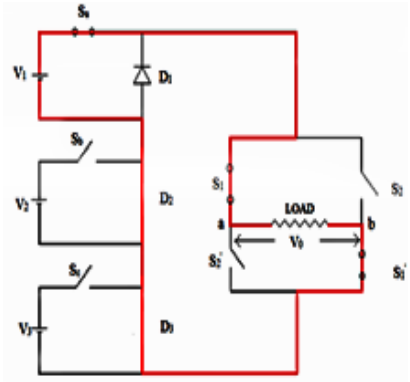

Fig.2. Mode 1 circuit operation

Linking the voltage source V_1 to the load, the swititches S_a, S_1, S_1' are turned on, the current flows from source V_1, S_a, S_1, load, S_1' and back to the source through the diodeD_2 and D_3 as shown in Fig. 2.

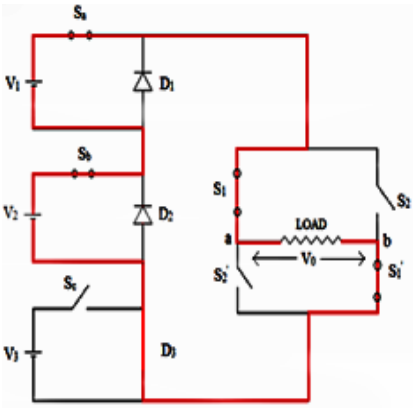

Fig.3. Mode 2 circuit Operation

Linking the voltage sources (V_1+V_2) to the load, the switches S_a, S_b, S_1, S_1' are turned on, the current flows from source (V_1+V_2), S_a, S_1, load, S_1' and back to the source through the doide D_3 and D_2 as in the fig. 3

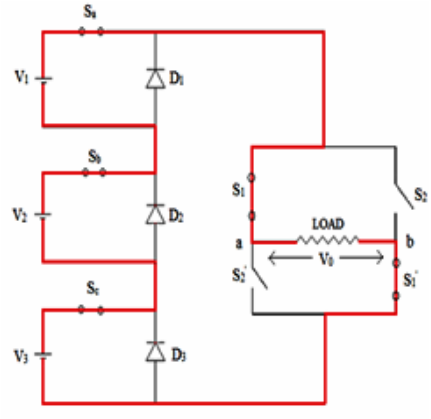

Fig.4. Mode 3 Circuit Operation

Linking the voltage sources (V_1+ V_2+ V_3) to the load, the switches S_a, S_b, S_c, S_1, S_1' are turned on, the current flows from sources (V_1+ V_2+ V_3), S_a, S_1, load, S_1' and back to the source as depicted in Fig. 4.

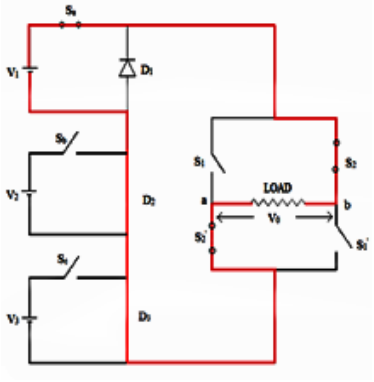

Fig.5. Mode 4 Circuit Operation

Linking the voltage source to produce $-V_1$ across the load, the switches S_a, S_2, S_2' are turned on, the current flows from source V_1 , S_a, S_2, load, S_2' and back to the source through the doides D_2 and D_3 as shown in the fig. 2.6. Linking the voltage sources to produce $-(V_1+V_2)$ across the load, the switches S_a, S_b, S_2, S_2' are turned on, the current flows from sources (V_1+V_2), S_a, S_2, load, S_2' and back to the source through the doide D3 and D2 as shown in the fig. 2.7. across the load, the switches S_a, S_b, S_2, S_2' are turned on, the current flows from sources (V_1+V_2), S_a, S_2, load, S_2' and back to the source through the doide D3 and D2 as shown in the fig. 5. The proposed topology synthesizes rectified multilevel dc-link voltage through a series of sub multilevel cells and alternated to produce unfolded multilevel waveform across an H-bridge inverter. Few sub cells are required to produce more number of levels by holding unequal voltage ratios in this structure.

Table 1. Switching strategy

Level	S_a	S_b	S_c	S_1	S_1'	S_2	S_2'
$+V_{dc}$	1	1	1	1	1	0	0
$+2V_{dc}/3$	1	1	0	1	1	0	0
$+V_{dc}/3$	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0
$-V_{dc}/3$	1	0	0	0	0	1	1
$-2V_{dc}/3$	1	1	0	0	0	1	1
-Vdc	1	1	1	0	0	1	1

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III. IMPROVED PWM TECHNIQUE

PWM techniques are used for controlling the output voltage and frequency of the inverter. Conventional PWM techniques like sinusoidal PWM or MCPWM suffers with higher Total Harmonic Distortion (THD) and lower fundamental voltage. This chapter proposes a novel carrier based technique that offers enhanced fundamental voltage with reduced THD.

A. Multi career PWM

In this PWM technique, the triangular carrier signal is compared with the reference sinusoidal signal to produce the PWM signal. The main disadvantages of this PWM technique are the higher THD, lower fundamental voltage and more switching losses. The carrier signal and the PWM signal is shown in the Fig 6.

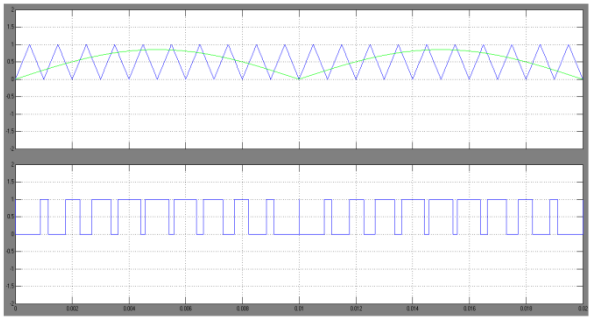

Fig.6. Carrier and PWM Signal

The PWM techniques include Phase Disposition (PD) PWM, Phase Opposition, Disposition (POD) PWM, Alternative Phase Opposite Disposition (APOD) PWM, Carrier Overlapping (CO) PWM, Phase Shift (PS) PWM and also Variable Frequency Carrier Band (VFCB) PWM.

B. 60˚ PWM Technique

In this technique, the switches are held on continuously for the period from 60˚ to 120˚. The pulse width from 60˚ to 120˚ doesn't have significant variation with change in modulation index. This technique results in enhanced fundamental voltage, reduced THD and reduced switching losses. With this technique, the triplen harmonics are eliminated in phase PWM inverters.

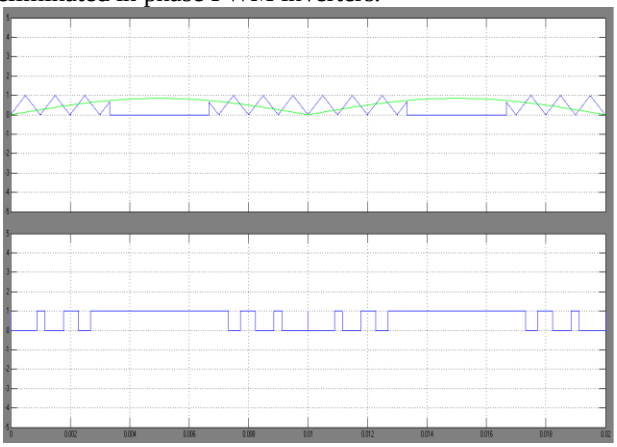

Fig.7. Carrier and PWM Signal

Table.2. Comparison between proposed PWM and MCPWM in terms of Fundamental output voltage

M_a	60˚ PWM (V)	MCPWM (V)
1	305.4	298.8
0.98	303	292.6
0.96	300.5	286.4
0.94	298.3	280.3
0.92	296.4	274.7
0.9	294.7	269.2
0.88	292.9	263.7
0.86	290.4	257.4
0.84	287.7	251
0.82	285.2	244.7

This chapter provides an insight analysis towards the conventional PWM methods in terms of switching, fundamental output voltage and distortion. Based on this, a new PWM technique called 60˚ PWM that reduces the switching loss at the verge of the reference sine wave in the carrier. This proposed scheme projects results in enhanced fundamental output voltage, reduced THD and reduced switching loss.

Table. 3. Comparison between proposed PWM and MCPWM in terms of THD

M_a	60˚ PWM (%)	MCPWM (%)
1	16.07	17.93
0.98	16.3	19.09
0.96	16.47	20.01
0.94	16.63	20.78
0.92	16.92	21.53
0.9	17.19	22.12
0.88	17.42	22.52
0.86	18.16	23.14
0.84	19.03	23.65
0.82	19.82	23.94

IV. RESULTS AND DISCUSSION

Having a detailed introduction and complete review from preceding chapters, one need study through simulation for understanding. In this chapter, the MCPWM and the proposed topology are simulated in MATLAB. A seven level output is considered for study. Specifications of simulations results presented are V_1: V_3=1:1:1, Resistive load=100Ω.

A. *Multi career PWM*

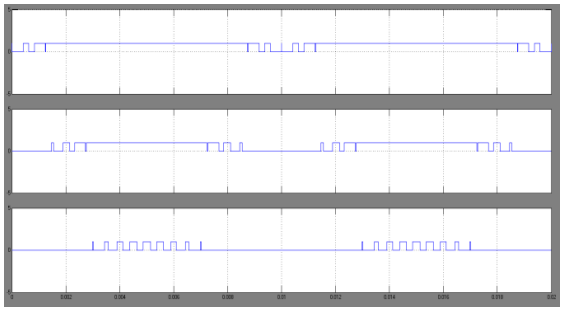

Fig.8. Pulse Pattern

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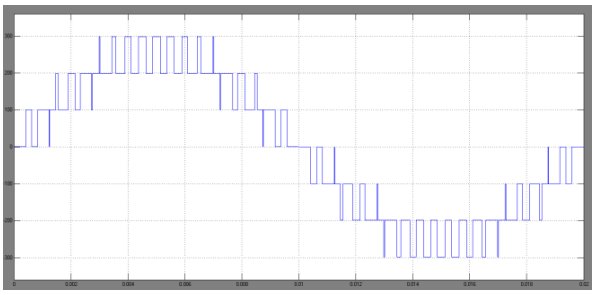

Fig.9. Output Voltage

The pulse pattern of multi career PWM signal is shown in fig.8 and fig.9 shows the output voltage signal. The fig.10 illustrates the voltage spectrum of multi career signal

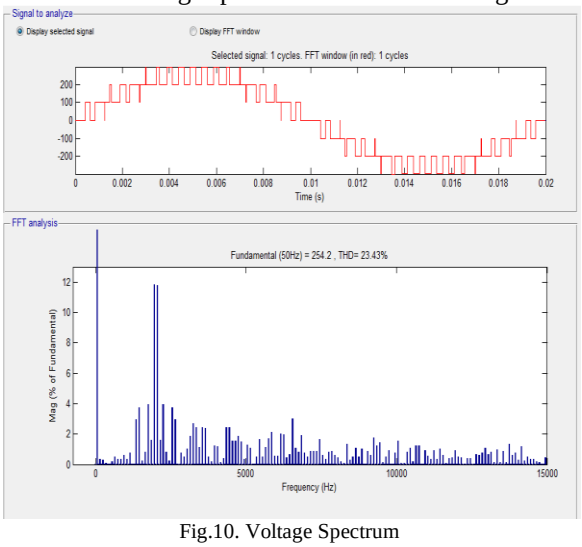

Fig.10. Voltage Spectrum

B. *60˚PWM* Technique

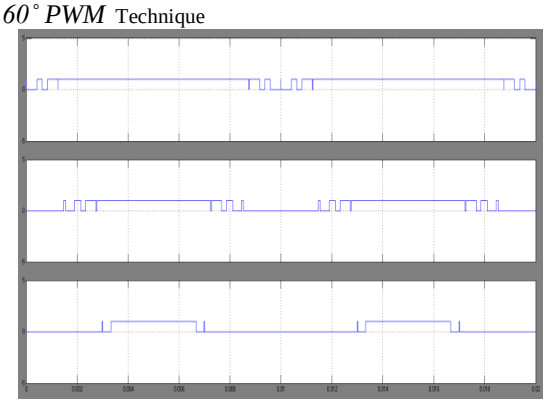

Fig.11. Pulse Pattern

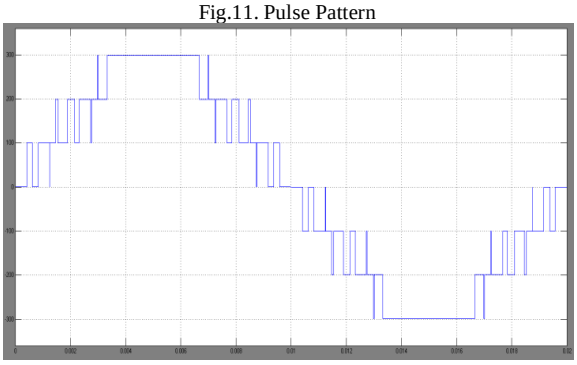

Fig.12. Output Voltage

The pulse pattern of 60°PWM technique signal is shown in fig.11 and fig.12 demonstrates the output voltage signal of 60°PWM technique signal.

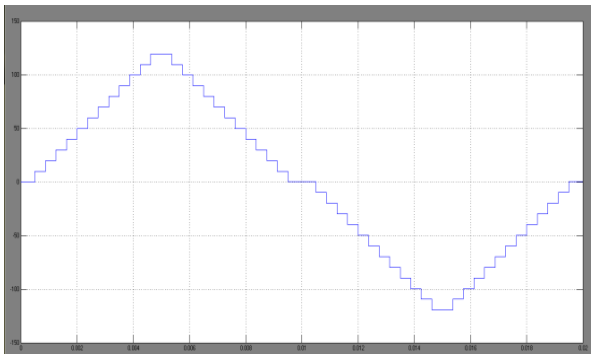

Fig.13. 25 level inverter Output voltage

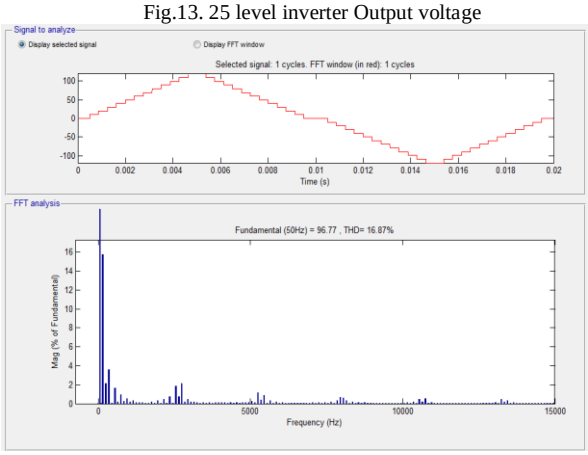

Fig.14. Voltage Spectrum

The fig.14 demonstrates the 25 level inverter output voltage signal and fig.15 shows the voltage spectrum.

V. CONCLUSION

This project has proposed new multilevel inverter topology and new modulation technique. The whole reported has successfully projected the "multilevel inverter" as separate research topic. In this project work, the most actively developed and widely used multilevel topologies like cascaded multilevel inverter, diode-clamped multilevel inverter; multilevel dc-link inverters are studied. Based on the knowledge gained from literature survey, a modified multilevel inverter with 60˚ PWM switching strategy has been simulated. The proposed type utilizes only seven switches to synthesize seven levels.

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