

A Novel Transformer less Interleaved High Step-Down Conversion Ratio DC-DC Converter with Low Switch Voltage Stress

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Abstract: A novel transformer less interleaved high step-down conversion ratio dc-dc converter with low switch voltage stress has been presented. In this converter, two input capacitors are series-charged by the input voltage and parallel discharged by a new two-phase IBC for providing a much higher step-down conversion ratio without adopting an extreme short duty cycle. Based on the capacitive voltage division, the main objectives of the new voltage-divider circuit in the converter are both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches. As a result, the presented converter topology possesses the low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. Moreover, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. Here interleaved buck converter and its operation are discussed. Also comparisons with conventional interleaved buck converter and simulation results are included.

Keywords: DC-DC Converter, MOSFETs, buck converter.

1. INTRODUCTION

In applications where non-isolation, step-down conversion ratio, and high output current with low ripple are required, an interleaved buck converter (IBC) has received a lot of attention due to its simple structure and low control complexity[1]. However, in the conventional IBC shown in Fig. 1.1, because active switch devices suffer from the input voltage, high voltage devices rated above the input voltage should be applied. High-voltage-rated devices are generally with poor characteristics such as high cost, large ON-resistance, large voltage drop, severe reverse recovery, etc. These limit the switching frequency of the converter and impact the power density improvement. For high-input and low-output voltage regulation applications, pursuing higher power density and better dynamics, it is required operating at higher switching frequencies that will increase both switching and conduction losses consequently, the efficiency is further deteriorated. Also, it experiences an extremely short duty cycle in the case of high input and low-output voltage applications. To deal with a small duty cycle of the IBC in high-input and low-output voltage regulation applications, a new extended duty ratio multiphase (Extended-D) topology has been proposed. The two phase extended duty ratio IBC is shown in Fig. 1.2. Extended duty ratio (ExtD) mechanisms are very efficient input voltage dividers which reduce the switching voltage and associated losses[2]. However, the voltage stress of the input switch devices remains rather high.

DC converter with low switch voltage stress is proposed. In the presented converter, two input capacitors are series-charged by the input voltage and parallel discharged by a new two-phase IBC for providing a much higher step-

down conversion ratio without adopting an extreme short duty cycle. Based on the capacitive voltage division, the main objectives of the new voltage-divider circuit in the converter are both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches.

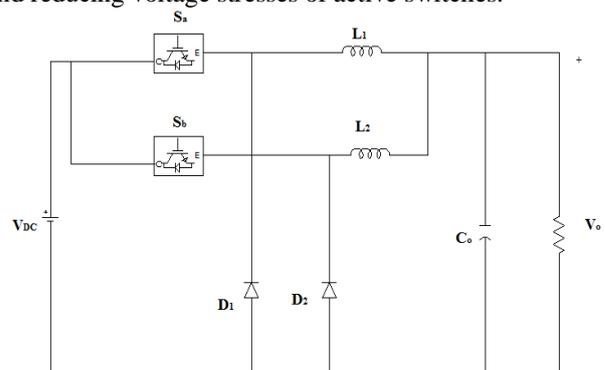


Fig.1.1. Conventional interleaved buck converter

As a result, the proposed converter topology possesses the low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. Moreover, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. The remaining contents of this report are organised as follows. First, the novel circuit topology and operation principle are discussed. Then, the corresponding steady state analysis is made to provide some basic converter characteristics.

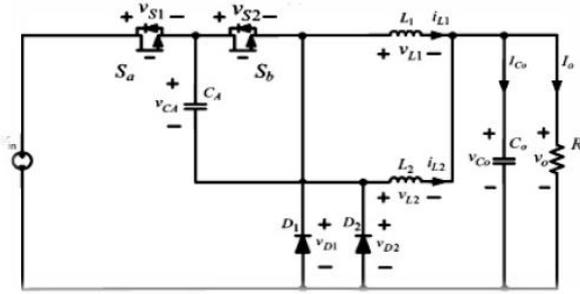


Fig 1.2 The two phase extended duty ratio IBC

2. OPERATING PRINCIPLE

The presented novel transformer less IBC is shown in Fig. 2.1 The presented converter consists of two inductors, four active power switches, two diodes, and four capacitors. The main objectives of the four capacitors are twofold. First, they are used to store energy as usual. Second, based on the capacitive voltage division principle, they are used to reduce the voltage stress of active switches as well as to increase the step-down conversion ratio. Basically, the operating principle of the presented converter can be classified into four operation modes. The interleaved gating signals with an 180 phase shift as well as some key operating waveforms are shown in Fig. 2.3. As the main objective is to obtain a high step-down conversion ratio and as such characteristic can only be achieved when the duty cycle is less than 0.5 and in CCM, hence the steady state analysis is made only for this case. However, in DCM, as there is not enough energy transfer from the blocking capacitors to the inductors, output capacitors, and load side, and as, consequently, it is not possible to get the charge balance of the blocking capacitor, then the nice automatic uniform current sharing property will be lost, and additional current-sharing control between phases should be included under this condition.

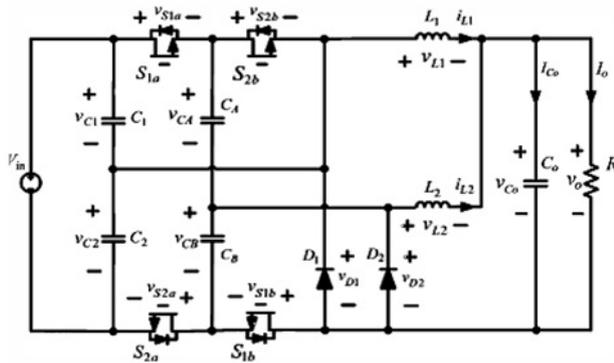


Fig 2.1 Proposed IBC

2.1 Operation Modes

2.1.1 Mode 1:[to-t1]

During this mode, S1a, S1b, and D1 are turned on, while S2a, S2b, and D2 are turned off. The corresponding equivalent circuit is shown in Fig. 2.2(a). From Fig. 2.2(a), one can see that, during this mode, current i_{L1} freewheels through D1, and L1 is releasing energy to the output load. However, current i_{L2} provides two separate current paths through CA and CB. The first path starts from C1, through S1a, CA, L2, CO and R, and D1 and then back to C1

again. Hence, the stored energy of C1 is discharged to CA, L2, and output load. The second path starts from CB, through L2, CO and R, and S1b and then back to CB again. In other words, the stored energy of CB is discharged to L2 and output load. Therefore, during this mode, i_{L2} is increasing, and i_{L1} is decreasing, as can be seen from Fig. 2.2(a). Also, from Fig. 2.2(a), one can see that V_{C1} is equal to V_{CA} plus V_{CB} due to conduction of S1a, S1b, and D1. Since $V_{C1} = V_{in}/2$ and $V_{CA} = V_{CB} = V_{C1}/2 = V_{in}/4$, one can observe from Fig. 2.2(a) that the voltage stress of D2 is equal to $V_{CB} = V_{in}/4$ and the voltage stresses of S2a and S2b are clamped to $V_{C2} = V_{in}/2$ and $V_{C1} = V_{in}/2$, respectively. The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = -V_{C0} \quad (2.1)$$

$$L_2 \frac{di_{L2}}{dt} = V_{C1} - V_{CA} - V_{CB} = V_{CB} - V_{C0} \quad (2.2)$$

$$(C_1 + C_2) \frac{dV_{C1}}{dt} = -i_{CA} \quad (2.3)$$

$$C_A \frac{dV_{CA}}{dt} = i_{L2} + i_{CB} \quad (2.4)$$

$$C_B \frac{dV_{CB}}{dt} = i_{CA} - i_{L2} \quad (2.5)$$

$$C_0 \frac{dV_{C0}}{dt} = i_{L1} + i_{L2} - \frac{V_{C0}}{R} \quad (2.6)$$

2.1.2 Mode 2:[t1-t2]

During this mode, S1a, S1b, S2a, and S2b are turned off. The corresponding equivalent circuit is shown in Fig. 2.2(b). From Fig. 2.2(b), we can see that both i_{L1} and i_{L2} are free wheeling through D1 and D2, respectively. Both V_{L1} and V_{L2} are equal to V_{C0} , and hence, i_{L1} and i_{L2} decrease linearly. During this mode, the voltage across S1a, namely V_{S1a} , is equal to the difference of V_{C1} and V_{CA} , and V_{S1b} is clamped at V_{CB} . Similarly, the voltage across S2a, namely V_{S2a} , is equal to the difference of V_{C2} and V_{CB} , and V_{S2b} is clamped at V_{CA} . The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{C0} \quad (2.7)$$

$$L_2 \frac{di_{L2}}{dt} = V_{C0} \quad (2.8)$$

$$(C_1 + C_2) \frac{dV_{C1}}{dt} = 0 \quad (2.9)$$

$$C_A \frac{dV_{CA}}{dt} = 0 \quad (2.10)$$

$$C_B \frac{dV_{CB}}{dt} = 0 \quad (2.11)$$

$$C_0 \frac{dV_{C0}}{dt} = i_{L1} + i_{L2} - \frac{V_{C0}}{R} \quad (2.12)$$

2.1.3 Mode 3:[t2-t3]

During this mode, S2a, S2b, and D2 are turned on, while S1a, S1b, and D1 are turned off. The corresponding equivalent circuit is shown in Fig. 2.2(c). From Fig. 2.2(c), we can see that, during this mode, current i_{L2} is

freewheeling through D2, and L2 is releasing energy to the output load. However, current i_{L1} provides two separate current paths through CA and CB. The first path starts from C2, through L1, C0 and R, D2, CB, and S2a and then back to C2 again. Hence, the stored energy of C2 is discharged to CB, L1, and output load. The second path starts from CA, through S2b, L1, C0 and R, and D2 and then back to CA again. In other words, the stored energy of CA is discharged to L1 and output load. Therefore, during this mode, i_{L1} is increasing, and i_{L2} is decreasing, as can be seen from Fig. 2.2(c). Also, from fig. 2.2(c), we can see that V_{C2} is equal to V_{CA} plus V_{CB} due to conduction of S2a and S2b. Since $V_{C2} = V_{in}/2$ and $V_{CA} = V_{CB} = V_{C2}/2 = V_{in}/4$, we can observe from Fig. 2.2(c) that the voltage stress of D1 is equal to $V_{CA} = V_{in}/4$ and the voltage stresses of S1a and S1b are clamped to $V_{C1} = V_{in}/2$ and $V_{CB} = V_{in}/4$, respectively. The corresponding state equations are given as follows:

$$L1 \frac{di_{L1}}{dt} = V_{in}v_{C1} - v_{CB} - v_{C0} = v_{CA} - v_{C0} \quad (2.13)$$

$$L2 \frac{di_{L2}}{dt} = v_{C0} \quad (2.14)$$

$$(C1 + C2) \frac{dv_{C1}}{dt} = i_{CB} \quad (2.15)$$

$$C_A \frac{dv_{CA}}{dt} = i_{CB}i_{L1} \quad (2.16)$$

$$C_B \frac{dv_{CB}}{dt} = i_{CA} + i_{L1} \quad (2.17)$$

$$C_0 \frac{dv_{C0}}{dt} = i_{L1} + i_{L2} \frac{v_{C0}}{R} \quad (2.18)$$

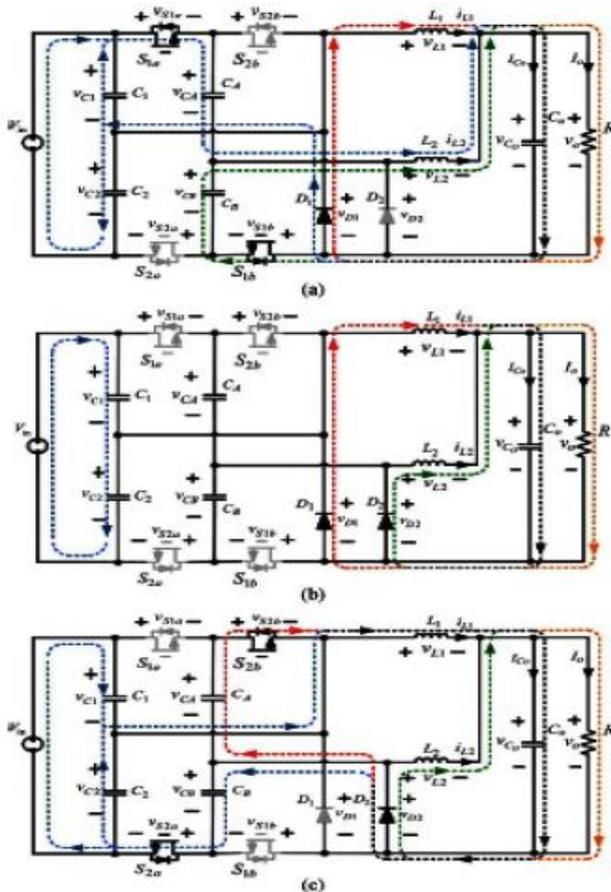


Fig 2.2 Mode of operation

2.1.4 Mode 4:[t3-t4]

In this mode S1a, S1b, S2a, and S2b are turned off. The equivalent circuit is same as Fig.2.2(b), and its operation is the same as that of mode 2. From the key operating waveforms of the presented converter shown in Fig.2.3 we can see the low voltage stress characteristic of four active switches and two diodes as well as the uniform current sharing

Summary

The four operating modes of the interleaved buck converter were explained. The equivalent circuit and corresponding waveforms were analysed. The voltage stress of four switches and two diodes are found to be low

3. DESIGN AND RESULT

Simulation Study

Simulation is performed with 400-V input. The switching frequency is chosen to be 40 kHz, both duty ratios of (S1a, S1b) and (S2a, S2b) are equal to 0.25. Due to the low switch voltage stress of the presented converter, three power MOSFETs with a rating of 250 V and one power MOSFET with a rating of 150 V and are used. Similarly, two diodes with low forward voltage drop are taken. The interleaved structure can effectively increase the switching frequency and reduce the output current ripples as well as the size of the energy storage inductors. Fig. 3.1 shows the simulated circuit in matlab. The simulated gate pulse V_{g1} , V_{g2} , I_{L1} , I_{L2} , V_{d1} , V_{d2} , V_{s1a} , V_{s2b} are shown in Fig 3.2 respectively

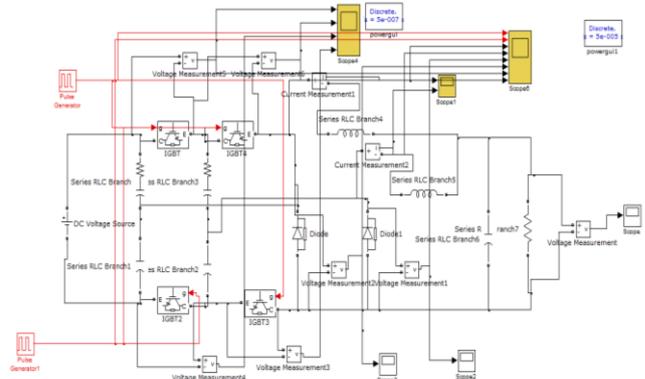


Fig 3.1 Simulated Proposed IBC

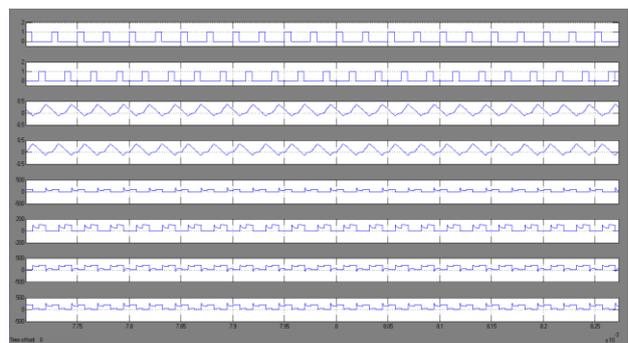


Fig 3.2 Output Waveforms V_{g1} , V_{g2} , I_{L1} , I_{L2} , V_{d1} , V_{d2} , V_{s1a} , V_{s2b} are shown in Fig 3.2 respectively

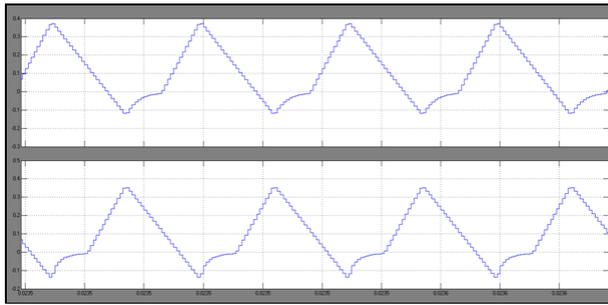


Fig 3.3 IL1&IL2

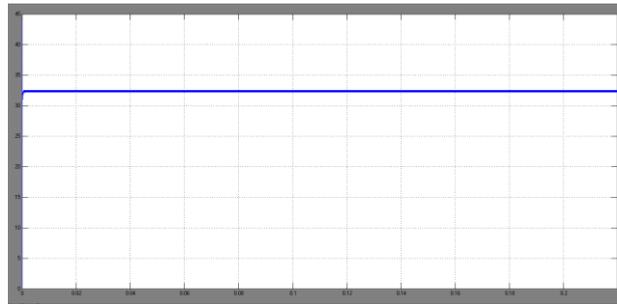


Fig 3.4 Output Voltage

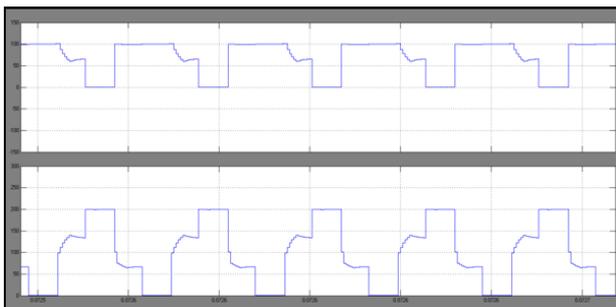


Fig 3.5 Voltage stress across switch

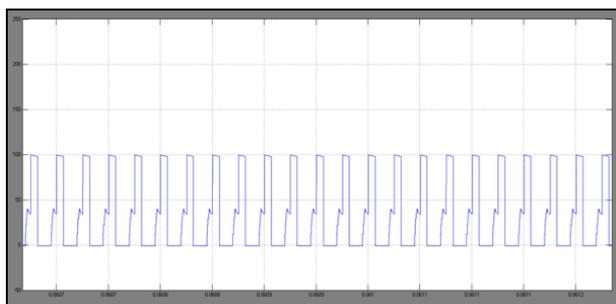


Fig 3.6 Switching stress across diode

4. CONCLUSION

A new IBC is presented in this paper. While keeping the good characteristics of the IBC introduced in, it has a more simple structure. The main advantage of the proposed IBC is that since the voltage stress across active switches is half of the input voltage before turn-on or after turn-off when the operating duty is below 50%, the capacitive discharging and switching losses can be reduced considerably. In addition, since the voltage stress of the free wheeling diodes is half of the input voltage in the steady state and can be quickly reduced below the input voltage during the cold startup, the use of lower voltage-rated diodes is allowed. Thus, the losses related to the

diodes can be improved by employing schottky diodes that have generally low breakdown voltages, typically below 200V. From these results, the efficiency of the presented IBC is higher than that of the conventional IBC and the improvement gets larger as the switching frequency increases. These are verified with the simulation results. Moreover, it is confirmed that the proposed IBC has a higher step-down conversion ratio and a smaller inductor current ripple than the conventional IBC. Therefore, the presented IBC becomes attractive in applications where non isolation, step-down conversion ratio with high input voltage, high output current with low ripple, higher power density, and low cost are required.

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