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Switched Capacitor Based Multilevel Inverter Topology Compatible with Multiple Inputs

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Abstract: A switched capacitor based multilevel inverter employing asymmetric source configuration is proposed. Multilevel inverters are mainly used to improve the harmonic profile of the output by increasing the number of levels. Due to the advancement in renewable energy, asymmetrical DC voltage sources are more common. The significant reduction in switch count of multilevel inverters has served as the greatest advantage over years. Various modulation schemes have been proposed in the literature to enhance the performance of multilevel inverters. This include Sinusoidal PWM (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE) etc. The switching strategies used for the control of switches influence the harmonic content of output voltage. Most of the modulation techniques, however contributed less in reducing the distortion at the output. In order to control the noise signals, lower order harmonics should be controlled. A modified Reduced carrier PWM scheme is proposed to control the harmonic content of the output voltage and thereby reduce the Total Harmonic Distortion. The simulation of the proposed system is modelled and evaluated with desirable results in MATLAB/Simulink.

Keywords: Switched-capacitor, H-Bridge, multilevel inverter, high frequency inverter, Total Harmonic Distortion, Reduced carrier PWM

I.INTRODUCTION

The various strategies on deriving energy from renewables, the rapid advances in technology and the increasing environmental stress have made the renewable energy resources to meet the future energy needs. The availability of sources such as wind, solar, photovoltaic, biofuels, geothermal and hydel energy are important aspects of many nations' energy strategies. As many of these resources have attained economic viability, their adoption and integration into today's electricity networks is becoming increasingly widespread. The concern about the environment and the need of developing sustainable energy supplies, will enhance the use of renewable energy resources in electric power generation [1]. However, the sustainability of the available resources is a major factor to be considered and hence, the use of these resources have to be in the most efficient way. The available sources in an area can be integrated for generating power, so that these resources can share the available load. When the load cannot be met by a single source, the sources can be used in cascade for efficient power generation.

Among the renewable energy sources available, solar energy has been one of the most active research areas, both for grid connected and stand-alone applications. The rapid rate of growth in the solar energy generation is mainly due to different inverter topologies [2]. Inverters therefore play a crucial role in the power generation, distribution and transmission systems incorporating renewable sources. AC output voltage is created by switching the full bridge in an appropriate sequence. The inverter topologies can be mainly divided into two: single and multi-stage inverter. Though the single stage inverters are less complex, the efficiency is very less due to high rate of change of output voltage and increase in the harmonic contents. The multi-level inverters have replace the single stage inverter circuits due to their high voltage capability, low switching frequency, and low power losses. The conventional multilevel topologies include the diode clamped, flying capacitor, and cascaded H-bridge converters.

In the past, multilevel switching was achieved by phase shifting of multiple single level converter output voltage waveforms which are added together vectorically using series connected transformer windings [3]. As the number of levels increased it became difficult to realize the approach due to requirement of multiple transformer windings. The alternative solution was to replace the multi-winding transformers with multilevel dc bus. This was achieved by connecting several controllable cells in series on the base of a single device connection to get a multilevel source [4]. The result of this approach was the conventional neutral point clamped, flying capacitor and cascaded H bridge topologies. The main drawbacks were the increase in the number of switches and hence the switching losses as the levels increase. Hence newer topologies were developed in the literature to reduce the number of components and the losses associated with it.

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With increase in the number of voltage levels, output waveform has more steps which help in reducing the harmonic content in the output. However, as the number of output level increases, the component count also increases proportionately making the circuit complex and bulky. A T-type inverter topology have been developed that reduces the switch count, but it does not support asymmetric source configuration [5]. A new reversing voltage topology for multilevel inverters have been proposed, but it cannot be operated with different dc source magnitudes since additive and subtractive combinations of dc sources cannot be obtained [6]. A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters have also been proposed in the literature [7]. The problem associated with that circuit is that it cannot develop a zero level by itself.

Various modulation strategies are developed for multilevel inverters to reduce the harmonic distortion at the output. In order to control the acoustic noise, lower order harmonics should be controlled and to control the electro - magnetic interference, higher order harmonics has to be reduced [8]. The modulation techniques are selected based on the switching frequency. Common modulation techniques include sinusoidal PWM, Space vector modulation, space vector control, Selective Harmonic Elimination (SHE) etc. SHE is the method of determining suitable angle for semiconductor switches in the inverter, the predetermined angle should be less than 90 degree [9]. In SHE, for a (2m+1) level inverter only (m-1) number of harmonics can be controlled. A seven level inverter employing side voltage is controlled by a PI controller to avoid the input variations. A seven level inverter employing reduced carrier PWM scheme with the main aim of reducing lower order harmonics is proposed in this paper.

II. PROPOSED SYSTEM

A seven level inverter consisting of a front end DC-DC converter and a H-bridge inverter is proposed. The front end converter is capable of producing multiple levels at the DC bus which when cascaded with the H-bridge produces the corresponding bipolar levels and the zero level. The front end converter consist of a capacitor which is called as a switched capacitor. The switched capacitor in the converter circuit convert input voltage to integral multiple output levels. This is done by charging the capacitor to the input voltage first, and then connecting the input source and the capacitor in series to the dc bus. The common aspect of the circuit is the H-bridge inverter which is used at the output of the dc-dc converter. Therefore, the seven level output can be obtained with a lesser number of components as compared to the conventional seven level inverter topologies.

Multiple input sources can be used in cascade in the proposed seven level inverter. In conventional systems, if multiple sources are available, either the sources are to be connected in series or the inverters employing individual sources have to be connected in parallel to achieve higher voltage levels. When input sources are to be connected in series, it requires complex voltage balancing schemes and the rating of the switches have to be increased. Complex control algorithms have to be implemented when inverters are operated in parallel. Hence both the methods add up to increase in cost and reduces the efficiency of the system.

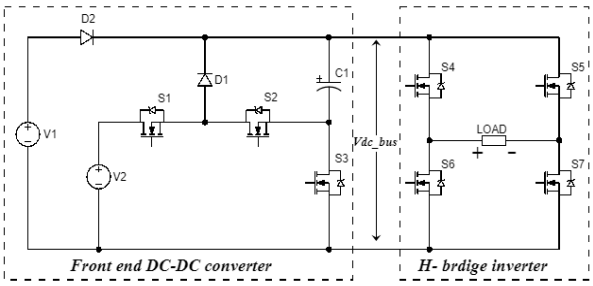

Fig. 1: Proposed seven level inverter

The proposed system consist of seven switches from S1 to S7 as shown in fig. 1. The front end DC-DC converter employs two input sources (V1 and V2), three switches (S1, S2 and S3), two diodes (D1 and D2), and a switching capacitor C1. The converter produces three output DC levels: V1, V2 and (V1+V2). The H bridge circuit at the output produces corresponding six bipolar level ±V1, ±V2 and ±(V1+V2) and the zero level, which is to be required as the output of the seven level inverter circuit.

III. OPERATION OF THE PROPOSED CIRCUIT

The proposed seven level inverter works in different operating modes to obtain different voltage levels at the output. The switches are switched sequentially to obtain the desired seven level output voltage.

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A. Output voltage ± V1: At first, in order to obtain +V1 at the output, the switches S3, S4 and S7 are turned on simultaneously so that the source V1 will be connected across the load. In the meantime the switching capacitor C1 gets charged to the input voltage V1. To obtain –V1, switch S3 is turned on along with S5 and S6.

B. Output voltage ± V2: The voltage level +V2 can be obtained by operating the switches S1, S4 and S7 and to obtain the corresponding negative part can be obtained by turning on S1 of the front end converter and S5 and S6 of the H- bridge inverter.

C. Output voltage ± (V1+V2): By turning on the switches S1, S2, S4 and S7 the output voltage level of (V1+V2) can be obtained as the capacitor was initially charged to V1 during the first stage. By the operation of S5 and S6 along with S1 and S2 voltage level – (V1+V2) can be obtained.

D. Output voltage = 0 V: To obtain zero level at the output after positive half cycle S4 alone of the H – bridge inverter is turned on. The diode of switch S5 act as the freewheeling diode during that time. Similarly after the negative half cycle switch S6 alone is turned on and the diode of S7 is used for freewheeling. During both the cycles switches of front end converter remain in their previous states. The switching logic of the seven level inverter circuit is shown in table 1.

TABLE 1 Switching logic for the seven level inverter

S1	S2	S3	S4	S5	S6	S7	Vout
0	0	1	1	0	0	0	0
0	0	1	1	0	0	1	V1
1	0	0	1	0	0	1	V2
1	1	0	1	0	0	1	V1+V2
0	0	1	0	1	1	0	-V1
1	0	0	0	1	1	0	-V2
1	1	0	0	1	1	0	-(V1+V2)
0	0	1	0	0	1	0	0

IV. MODULATION TECHNIQUE

Several modulation strategies can be adopted to realize the proposed seven level inverter. These strategies form the basic factor in determining the harmonic content in the output waveform. The modulation technique used to realize the proposed inverter aimed at reducing the lower order harmonics in the output waveform and thereby reducing the THD. Here a Reduced Carrier Pulse Width modulation with Unified logical expression technique is used. This method is one of the simplest PWM methods. Basic PWM method involve more number of carriers to obtain the switching pulses for the inverter switches. Moreover, conventional PWM schemes result in degraded line THD performance. The proposed method vary with the inverter topology as the logical expressions are not generalized. Based on the switching sequence of various switches the logical expressions for different switches are made. The system employs four carriers along with a unipolar reference in order to obtain the switching pulses for the seven switches.

The reduced carrier PWM scheme, as the name suggests use lesser number of carriers compared to the conventional PWM methods. The main advantage of the proposed scheme is that it topology independent, this switching logic can control any reduced switch count multilevel inverters, irrespective of the voltage source configuration. When the proposed topology is extended for higher levels, the reduced carrier PWM scheme offers less computational burden and improvement in line voltage THD. The turnaround time for implementing the proposed PWM scheme is less and remains almost same for different inverter topologies employing the same number of levels. Higher switching frequencies can be implemented with the proposed scheme because of its low computational burden. The switching signals for the different switches of the proposed inverter circuit is shown in fig. 2.

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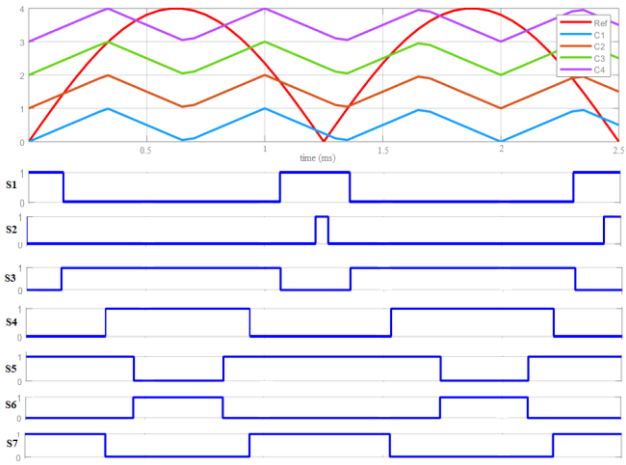

Fig. 2: Switching scheme of the seven level inverter

V. SIMULATION RESULTS

The proposed system is simulated in MATLAB/SIMULINK. The simulation model is shown in fig. 3.

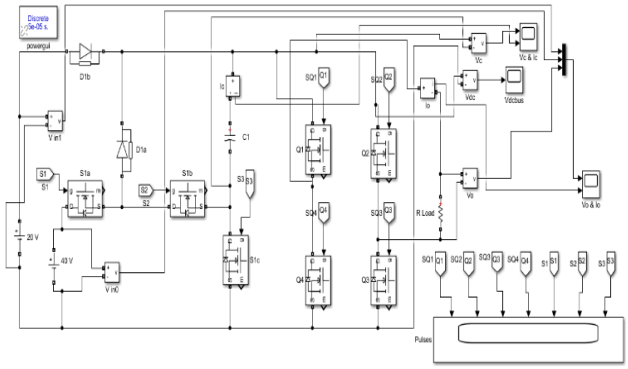

Fig. 3: Simulink model of the proposed system

The inputs to the system are 20V and 40V. The system is simulated for an output frequency of 400 Hz using the reduced carrier modulation technique. Seven output levels are obtained in the output waveform: 0 V, ±20 V, ±40 V and ±60 V. A 25Ω resistor is used as the load in the proposed system. As a resistive load is used the output current follows the output voltage waveform. The switching capacitor must be capable of charging to a voltage of V1, hence a 470 µF capacitor is used.

The voltage stress across the different switches of the front end dc-dc converter can be understood from the following waveforms (fig. 4). The switch voltage stress is found to be less, 24 V for S1, 20V for S2 and 40 V for S3.

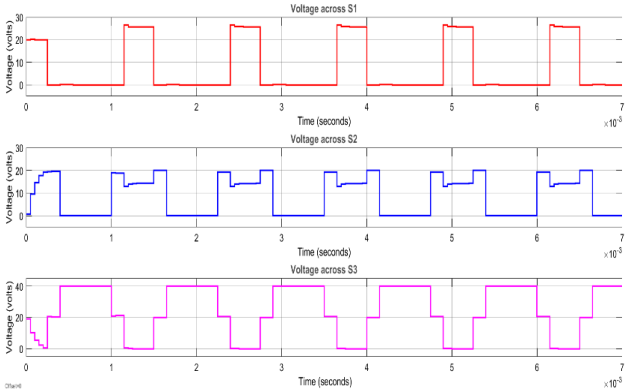

Fig. 4: Voltage waveform across converter switches

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The output voltage and current waveform of the seven level inverter is shown in fig. 5.

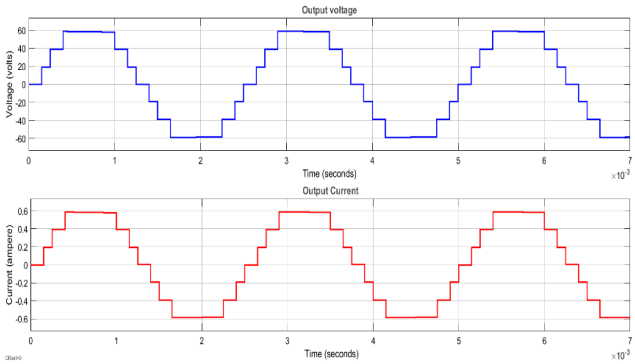

Fig. 5: Output voltage and current waveform

The dc bus voltage waveform is shown in fig. 6. With the help of switches S1, S2, S3 and the switching capacitor C1, it is possible to attain the dc voltage levels of 20V, 40V and 60V. The switching capacitor voltage and current waveforms are shown in fig. 7.

The switching capacitor plays the role of producing the output voltage level of 60 V. The capacitor charging and discharging characteristics determine the efficiency of the output voltage waveform. The ripples at the output can be minimized by properly choosing the capacitance value.

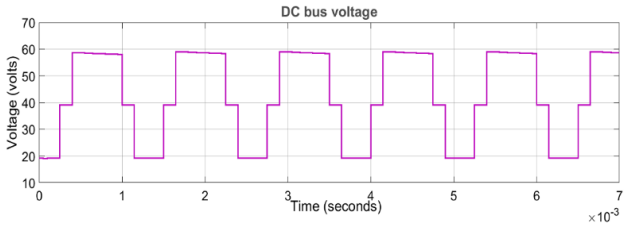

Fig. 6: DC bus voltage waveform

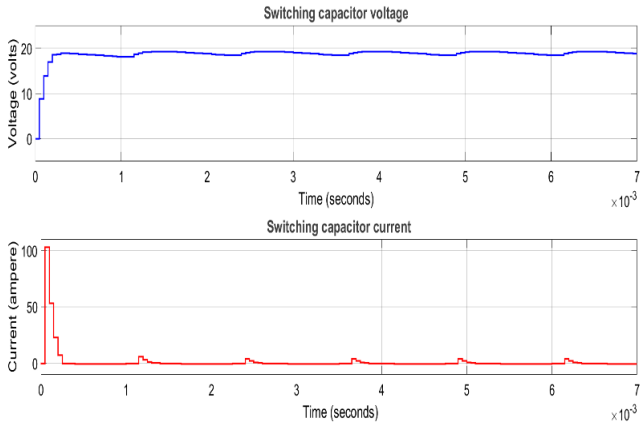

Fig. 7: Switched capacitor voltage and current waveform

The main advantage of the proposed seven level inverter employing reduced carrier PWM technique is the reduction in the harmonic content. The THD is found to be 4.53 % which is a much smaller value compared to conventional multilevel inverter topologies. It has been found that the lower order harmonics are having a less value and all the even order harmonics have been eliminated (fig. 8). This further contributed in the reduction of THD.

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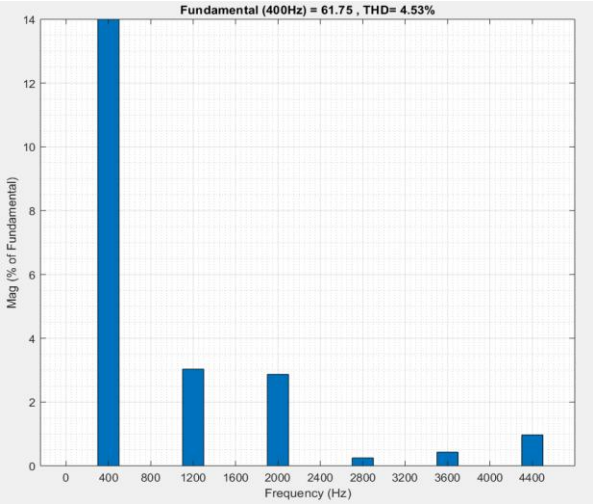

Fig. 8: THD of the output voltage

The analysis and simulation of the seven level inverter employing reduced carrier PWM method resulted in a higher efficiency of more than 90%.

VI. CONCLUSION

A new switched capacitor based seven level inverter employing reduced carrier PWM scheme is proposed here. The inverter is capable of operating with multiple sources. Such situations arise when large firms use different renewable sources for the electric power generation. As series connection of multiple sources is not used, the issue of voltage balancing can be eliminated. The high frequency of the output makes it possible to be employed with special applications such as aerospace. The reduced carrier PWM method with unified logical expressions helped in the proper switching of the components and made it possible to reduce the THD. The even order harmonics were completely eliminated and the lower order odd harmonics were minimized. If multiple sources are available, the system can be extended to obtain more levels and hence a more efficient output can be obtained.

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