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Design of Multistage Linear Feedback Shift Register Based Counters Using Cmos Logic Style

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Abstract: Linear-Feedback Register (LFSR) based counters are found to be suited for many applications which uses large arrays of counters and may also improve the performance compared with the traditional binary based counters. In order to decode the count order into binary, improved logic is needed which makes system-on-chip designs to be unfeasible. This paper presents a counter design supported by multiple LFSR stages that has the benefits of a single-stage LFSR but the essential decoding logic scales logarithmically with the number of stages as against exponentially with the number of bits with other methods. A four-stage four-bit LFSR based counter was designed and proof of concept was fabricated in 90nm CMOS technology and was characterized during a time-to-digital converter application at 800 MHz.

Keywords: Binary counters, decoding logic, event counters, Linear-Feedback Register (LFSR), single-photon detection

I.INTRODUCTION

A Linear-Feedback register (LFSR) is a register in which the input bit is a linear function of its previous state, the most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most frequently a register whose input bit is driven by the XOR of some bits of the general register value. The initial value of the LFSR is the seed, and since the operation of the register is deterministic, the stream of values produced by the register is totally determined by its present (or previous) state. Similarly, the register features a finite number of possible states, it should eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and features a very long cycle. LFSRs are mainly used in generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. The implementation of LFSR is common in hardware and software. The mathematics of a cyclic redundancy check, was to provide a fast check against transmission errors, are closely associated with those of an LFSR.

II.BACKGROUND

With recent advances in applications like single-photon detection, it's become necessary to implement an outsized number of arrayed counters in small areas. These include time-of-flight (TOF) ranging thorough cameras where counters are required to count clock cycles and also photon-counting cameras that count the amount of photons in an interval. Reducing the world consumed by the counter within the se applications is critical in increasing the amount of pixels in the cameras, as each camera pixel contains a separate counter. While linear-feedback shift registers (LFSRs) are typically used as pseudorandom number generators, it's been shown that they're also an efficient thanks to implement synchronous counters and are compatible to large arrayed designs, because the register can act as a serial readout mechanism.

LFSR counters are utilized in the CMOS pixel design and in single-photon detection arrays. The clock speed of an LFSR is independent of the amount of bits within the counter, and that they traverse all states within the state space except the all zero state. However, the count order of LFSRs is pseudorandom, so extra processing is required to decode the LFSR state into binary order. Three different techniques to decode the LFSR sequence into binary are compared within the iteration method, the direct lookup table (LUT) method, and a time-memory tradeoff algorithm. The iteration method iterates over the whole count sequence of the LFSR and compares each to the counter value. For an n-bit LFSR, this needs approximately $2n-1$ comparisons on the average. The direct LUT method instead uses an $n \times n$ LUT that directly decodes the LFSR state. The time-memory tradeoff algorithm introduced in combines both methods by storing 2(N/2) LFSR count values during a table and iterating over the LFSR sequence until the count value matches a worth within the table. The amount of iterations is then subtracted from the stored value to get the decoded value. Another algorithm supported discrete logarithms was introduced

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in and was adapted to be used with ring generator event counters.
Applications with large arrays require every cell within the array to be decoded to binary order for further processing, and for system-on-chip designs, it's necessary to perform this decoding on chip. This requirement dictates that the decoding logic must be integral and fast, since many conversions got to occur. However, all of the above-mentioned methods grow exponentially in either time or area with the dimensions of the LFSR. For single-photon detection applications, there are several samples of arrayed designs that might not be ready to be implemented with LFSR counters without prohibitively large integrated LUTs.
This paper proposes a replacement counter design supported multiple LFSR stages, which may be decoded with logic that grows logarithmically with the counter size instead of exponentially. While an easy concatenation of LFSR counters would cause a big performance reduction, almost like binary ripple counters, this paper introduces a way to distribute the ripple signal in time and compensates for this during a generalized decoding logic scheme. This paper also presents a symbol of concept implementation and characterization of this counter design during a 90-nm CMOS process. Throughout the rest of this paper, an n-bit LFSR are going to be mentioned as an n-LFSR

III.PROPOSED METHOD

A. Design of 4-bit adder

The general scheme of the counter design is shown in Fig. 1. There are M identical n-LFSR blocks that are controlled by an enable signal. When the (m − 1)th n-LFSR undergoes a specific state change, the enable signal is asserted so that the mth n-LFSR advances one state. This allows the entire M × n bit state space to be traversed. In large arrayed designs, the counter can also act as a high-speed serial readout chain. This is achieved with minimal additional logic that bypasses the LFSR feedback and ripple-carry blocks. The multistage counter scheme reduces the counter into M independent modules, allowing each n-LFSR to be decoded separately by an n×n bit LUT rather than an (M×n)×(M×n) bit LUT. For small n, the LUT can easily be implemented on chip.

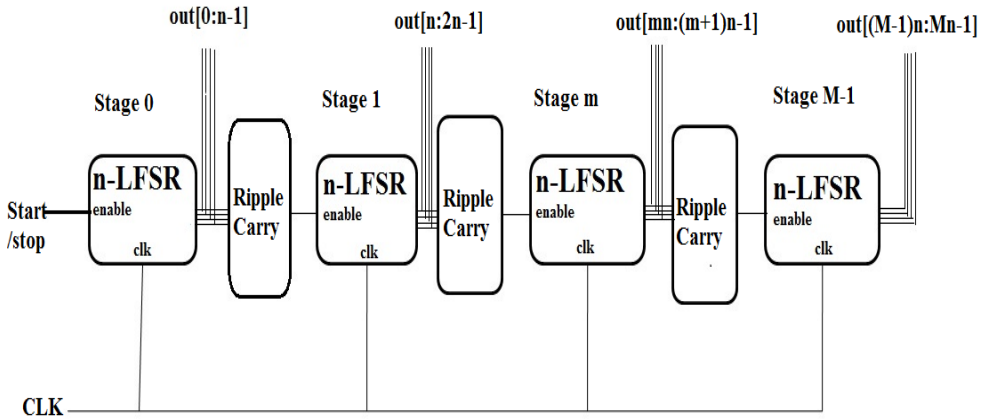

Fig.1 Block diagram of the multistage LFSR counter

Each stage of the counter is triggered once per period of the previous stage, so missing states from the LFSR sequence will cause large blocks of counter states to be missing from the counter state space. Thus, it's important that the n-LFSR is meant for a maximal length. The maximal sequence length of an n-LFSR is merely 2n − 1, so additional logic is required to include the missing state into the count sequence. This can be achieved using a NOR and XOR function to disable the feedback logic when the 0x000 …1 state is detected, as shown in Fig. 2(c). This sequence-extension logic extends the sequence length of the individual component LFSRs to 2n in order that the counter covers every state within the 2M×n state space. This also allows the multistage counter to be used in applications that require every state to be covered, such as self-starting counters, where traditional LFSRs would not be applicable

B.Reduced LFSR Using CMOS Logic
Several LFSR feedback styles exist, including many-to-one, one-to-many (alternatively known as Fibonacci and Galois LFSRs, respectively), and ring generators. Ring generators [depicted in Fig.2 (a)] are typically regarded as the optimal way to implement an LFSR, where the shift register forms a ring and taps form sub loops within the ring. However, the sequence-extension requires additional logic in the LFSR, dominating the critical path. Instead, many-to-one style LFSRs

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[Fig.2 (b)] are used, allowing the feedback logic and the sequence-extension logic to be combined into a single logic block for logic minimization as shown in Fig.2(c). The multistage counter allows flexibility in choice of the size of the n-LFSR, so that small single-tap LFSRs are preferentially

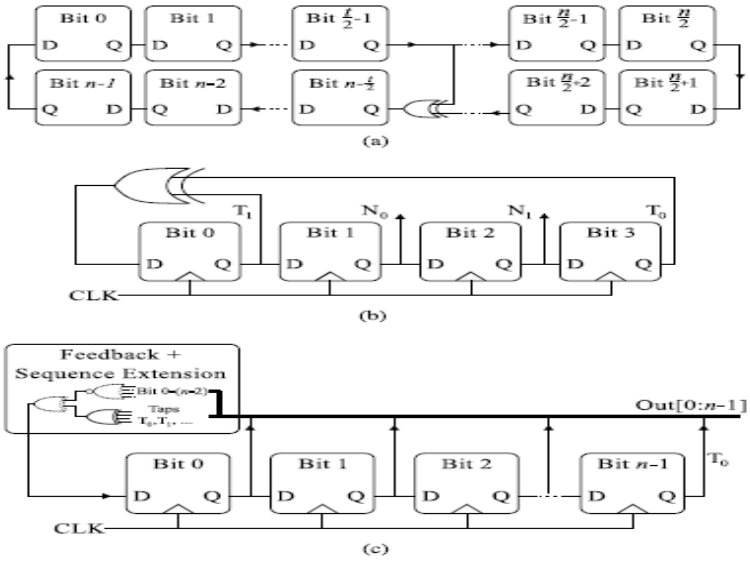

Fig.2(a) Structure of a conventional n-bit ring generator. 2(b) Structure of conventional many-to-one 4-LFSRs.2 (c) Structure of a proposed multistage n-LFSR block with sequence-extension logic (dotted components). The entire feedback block is implemented as a single logic block.Ripple-Carry Logic chosen.

A single-tap many-to-one LFSR is topologically indistinguishable from the corresponding ring generator.
Since the n-LFSR contains every state in the state space, the LFSR must include the 0b1111 … → 0b0111 … transition. This state is a Gray-code transition and occurs in every n-LFSR design, so it is an ideal ripple trigger transition. This sets the start of the n-LFSR sequence to 0b0111 … so that it is decoded by the decoding logic to 0x …00. If the counter was designed so that an LUT could directly decode every stage correctly in a single clock cycle, the ripple signal would need to propagate through every stage and detect if each stage will transition. Instead, to prevent the performance of the counter from decreasing with every extra stage added to the counter, the ripple signal only acts on the direct next stage and the ripple signal for the subsequent stages is carried to the next clock cycle. This distributes the transition edge over time and, for the m^{th} stage, adds an m clock cycle delay to the transition edge.

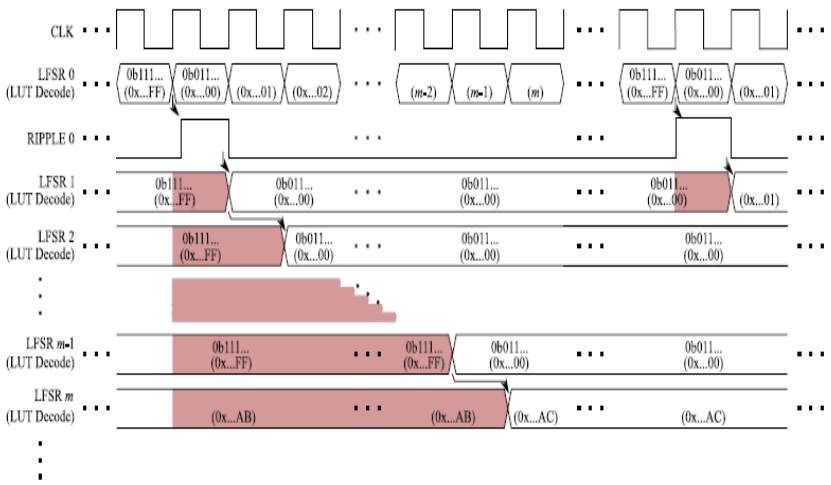

Fig.3 Timing diagram of the operation of the multistage LFSR counter

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Arrows show the operation of the ripple-carry logic. Highlighted states require further processing by the decoding logic. The counter timing diagram that demonstrates the operation of the ripple-carry logic is shown in Fig. 3. Each LFSR state is given as a binary value (0b …), whereas the state after decoding with an LUT (the LUT Decode signal) is the hex value in brackets (0x …) for each state. When LFSR 0 transitions from the 0b1111 … state to the 0b0111 … state, the RIPPLE 0 signal is generated. On the next clock edge, the RIPPLE 0 signal acts on LFSR 1 causing it to also undergo the 0b1111 … → 0b0111 … transition. This, therefore, also generates a ripple signal to act on LFSR 2 on the next clock edge. In this way, the ripple-carry logic causes the transition edge to be delayed one clock cycle per stage. The delayed transition causes an error triangle to form, shown by highlighted states in Fig. 3. These states are decoded incorrectly by the LUT and therefore need to be corrected with a minor amount of decoding logic in addition to the n × n bit LUT.

IV. RESULT AND SIMULATION

In this work, a comparison of the area, power consumption, and operating frequency of the implemented four-stage 4-LFSR to other state-of-the-art single-photon detection arrays is presented in Table I. This shows that the four-stage 4-LFSR compares well in terms of area to other single-photon sensor arrays, although in comparing area, it is important to note that the compared designs may include other circuitry within the stated area. The four-stage 4-LFSR also allows a much higher clock frequency than the reported counter operating frequencies of the other designs allowing the counter of the TDC to have a higher timing resolution.

A.125nm TECHNOLOGY

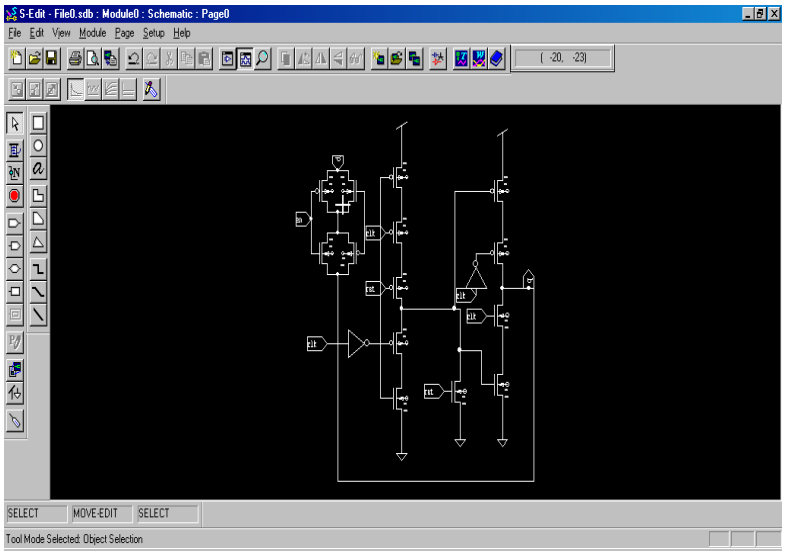

Fig 4 Schematic of dynamic logic circuit

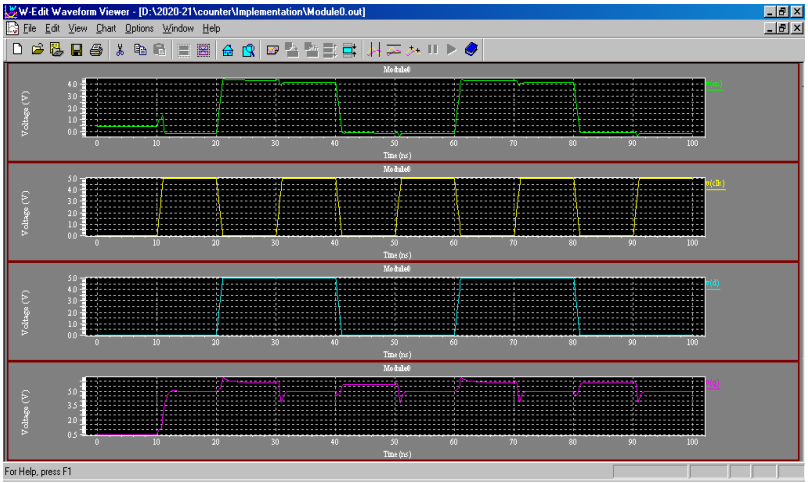

Fig.5 Simulation Output in dynamic logic

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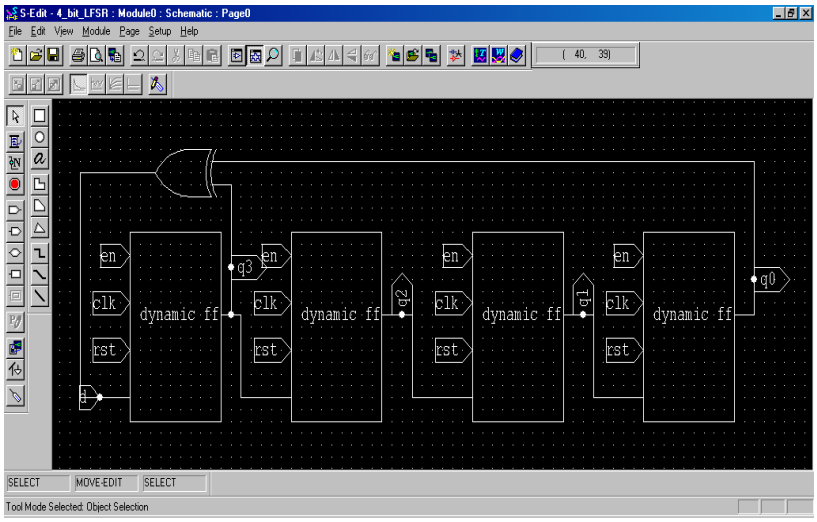

Fig 6 Schematic of 4-bit LFSR adder

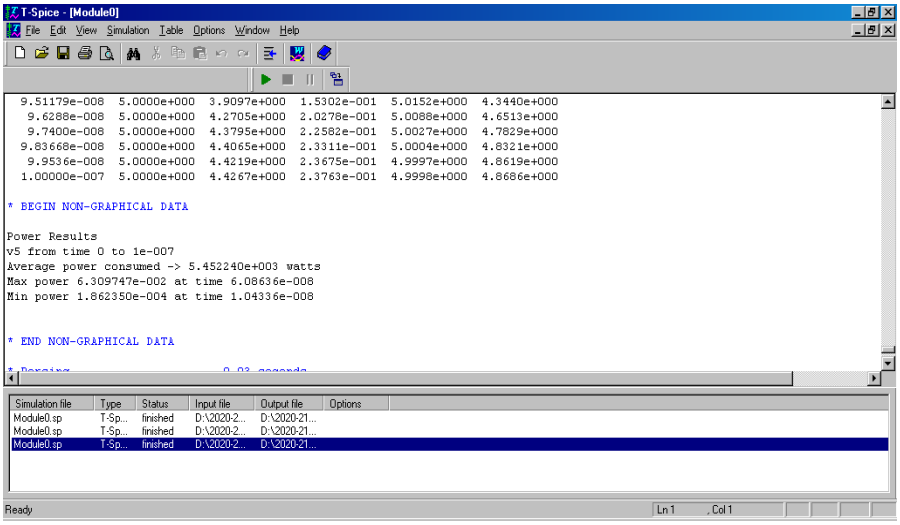

Fig.7 Output of Power

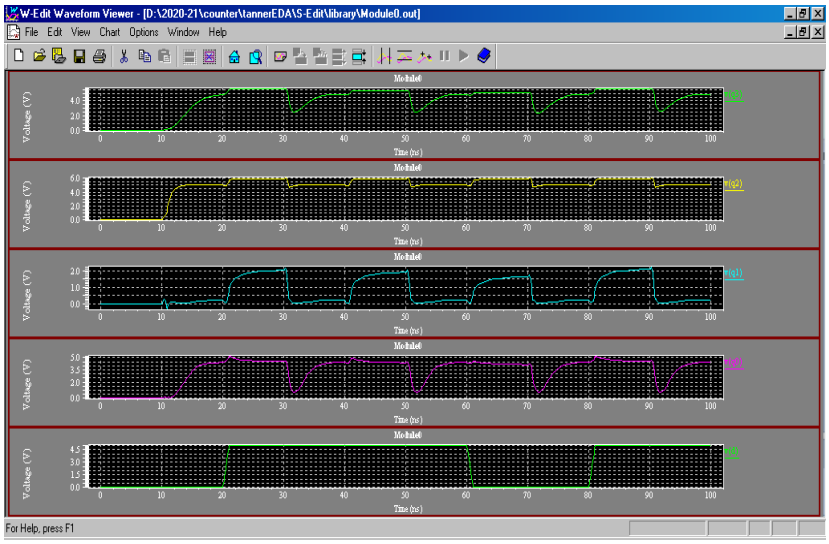

Fig.8 Simulation output

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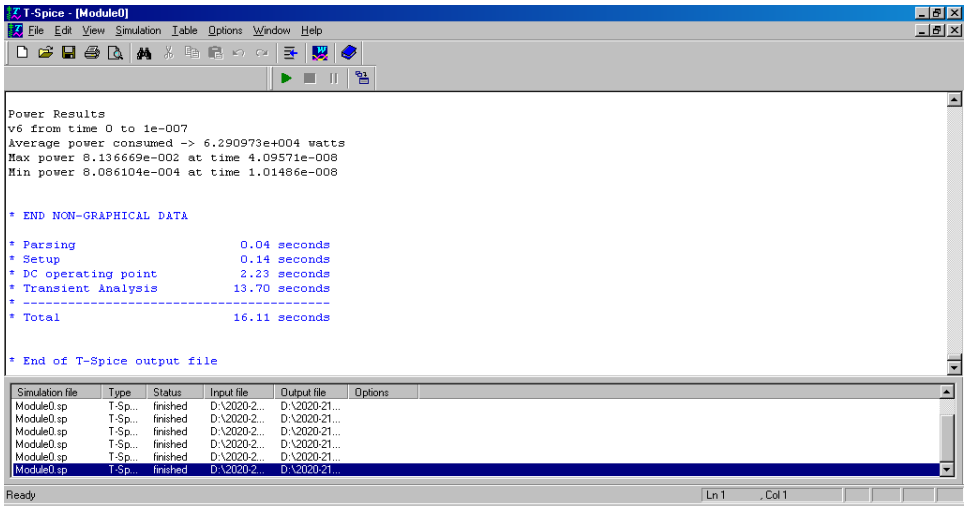

Fig.9 Delay output

B.90nm TECHNOLOGY

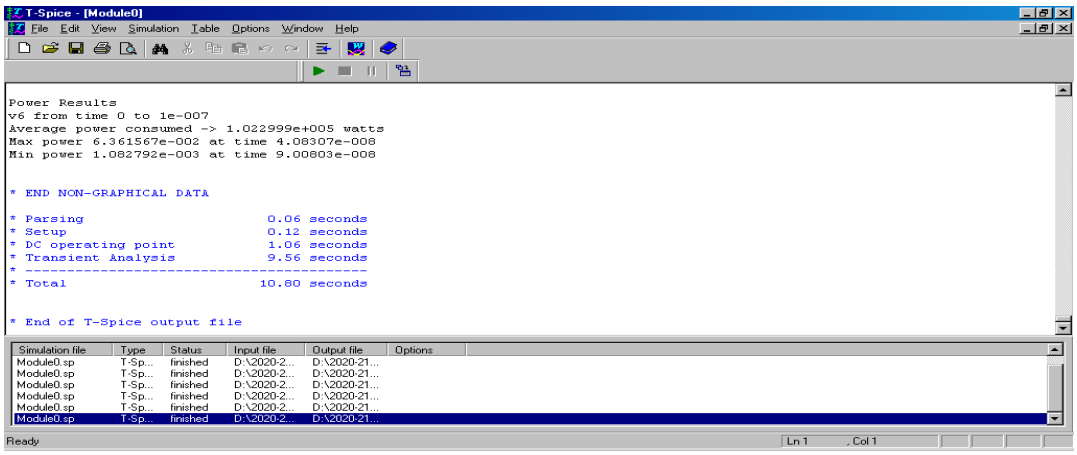

Fig.10 Delay output

TABLE I: COMPARISON TABLE

PARAMETERS	125nm	90nm
NUMBER OF MOSFET	194	194
POWER (W)	1.098	0.858
DELAY(S)	16.11	10.80

V. CONCLUSION AND FUTURE WORK

The continuous power consumption of the four-stage 4-LFSR is high compared with the power consumption of the other designs partially due to the usage of dynamic logic. However, the TDCs in these applications are typically operated at a low duty cycle. This paper was implemented in a 90-nm CMOS process as it is typical in single-photon detection applications. Extending this design to more advanced technology nodes for other applications would require care due to the dynamic logic style used. Dynamic logic is inherently more susceptible to noise than conventional logic techniques, and the increased PVT variation may cause further performance variability

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