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Low Power Decoder Enabled Pulsed Latch Based Bi-directional Shift Registers

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Abstract: Shift register are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. The proposed work uses a decoder enabled pulsed latch to design a low-power and area-efficient shift register. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal.The area and power consumption are reduced by replacing flip-flops with pulsed latches. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 16-bit shift register using pulsed latches was synthesized using Xilinx FPGA. The proposed shift register saves area and power compared to the conventional shift register with flip-flops. A 256bit Bi-Directional shift register was fabricated using a 65nm CMOS Process. It reduces area by 22.3% power consumption by 11.2% compared to low power area andshift register.

Keywords: Area efficient, Bi-Directional Shift, Flip flop, Pulsed clock, Pulsed latch.

I. INTRODUCTION

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the 'bit array' stored in it, 'shifting in' the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input [1]. More generally, a shift register may be multidimensional, such that its 'data in' and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register.

A. Flip-Flops for High-Performance and Low-Power Systems: [2]A Low-Power Double Edge-Triggered Flip-Flop with Transmission Gates and Clock GatingIn recent years, energy saving techniques have become critical in hardware designs, especially for mobile devices. This paper has reviewed several previous designs of double edge-triggered flip-flops, and has proposed a transmission-gate-based double edge-triggered flip-flop with a clock-gating function. Comparing to the previous work of double edge-triggered flip-flops, the proposed one saved 33.14% power on average (switching activity factor = 0-0.4) and it can save up to 97.85% power compared to conventional single edge triggered flip-flops when the input is idle. In addition, the proposed design also improved performance by reducing Clk-to-Q latency by 0.21 ns. [3] Activity-Sensitive Flip-Flop and Latch Selection for Reduced Energy This paper presents new techniques to evaluate the energy and delay of flip-flop and latch designs and shows that no single existing design performs well across the wide range of operating regimes present in complex systems. We propose the use of a selection of flip-flop and latch designs, each tuned for different activation patterns and speed requirements. We illustrateour technique on a pipelined MIPS processor datapath running SPECint95 benchmarks, where we reduce total flip-flop and latch energy by over 60% without increasing cycle time. [4] Comparative Analysis of Master–Slave Latches and Flip-Flops for High-Performance and Low-Power SystemsIn this paper, we propose a set of rules for consistent estimation of the real performance and power features of the flip-flop and master–slave latch structures. A new simulation and optimization approach is presented, targeting both high performance and power budget issues [5]. The analysis approach reveals the sources of performance and power-consumption bottlenecks in different design styles. Certain misleading parameters have been properly modified and weighted to reflect the real properties of the compared structures. Furthermore, the results of the comparison of representative master–slave latches and flipflops illustrate the advantages of our approach and the suitability of different design styles for high-performance and low-power applications. The rest of the paper is organized as follows: Section II describes the architecture of the bidirectional shift-register. Sec III presents the proposed decoder enabled bidirectional shift-register & section IV evaluates the result. Finally, conclusion are drawn in Section V.

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II. BIDIRECTIONAL SHIFT REGISTER

The N-bit bidirectional shift-register can be realized by connecting the N BD-PLs in series. Fig. 1 shows the schematic of the proposed bidirectional pulsed-latch (BD-PL). The differential data inputs from the left latch (DL and DL_b) are connected to the differential data outputs (Q and Qb) of the left latch. The differential data inputs from the right latch (DR and DR_b) are connected to the differential data outputs (Q and Qb) of the right latch.

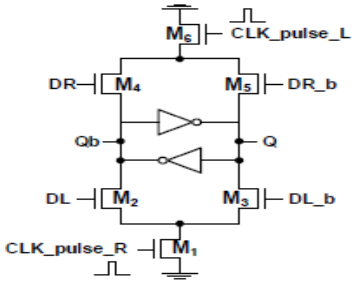

Fig. 1. Schematic of the proposed bidirectional pulsed-latch (BD-PL).

When the pulsed clock signal for right-shifting or left-shifting (CLK_pulse_R or CLK_pulse_L) is high, the latch data is updated to the left or right. Therefore, the BD-PL stores the left or right latch data according to CLK_pulse_R or CLK_pulse_L, respectively.

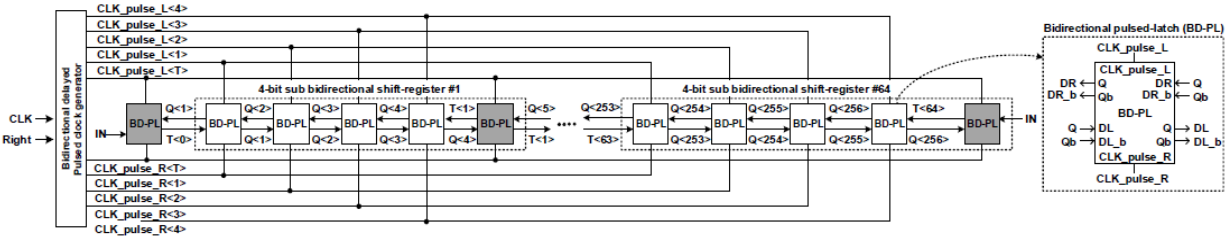

Fig. 2. Proposed 256-bit bidirectional shift-register using bidirectional pulsed-latches (BD-PL).

Fig. 2 shows the proposed 256-bit bidirectional shift-register using BD-PLs. It applies sub shift-registers and additional temporary latches to reduce the number of the pulsed clock signals [5]. It simplifies the block of the BD-PL omitting the complementary signals (Qb, DR_b, and, DL_b) to explain the operation easily. It consists of a bidirectional delayed pulsed clock generator, 64 4-bit sub bidirectional shift- registers, and an extra temporary latch. The extra temporary BD-PL is added in front of the bidirectional shift-register in order to store the input signal (IN) for right-shifting. The 4-bit sub bidirectional shift-register requires five BD-PLs to shift data right or left by using five pulsed clock signals for right-shifting (CLK_pulse_R<1:4> and CLK_pulse_R<T>) or five pulsed clock signals for left-shifting (CLK_pulse_L<1:4> and CLK_pulse_L<T>), respectively. In the 4-bit sub bidirectional shift-register #1, four BD-PLs store 4-bit data (Q<1>-Q<4>) and shift the 4-bit data right or left. The temporary BD-PL stores Q<4> or the first BD-PL data (Q<5>) of the next sub bidirectional shift-register. Exceptionally, in the sub bidirectional shift-register #64, the temporary BD-PL stores the input signal (IN) for left-shifting.

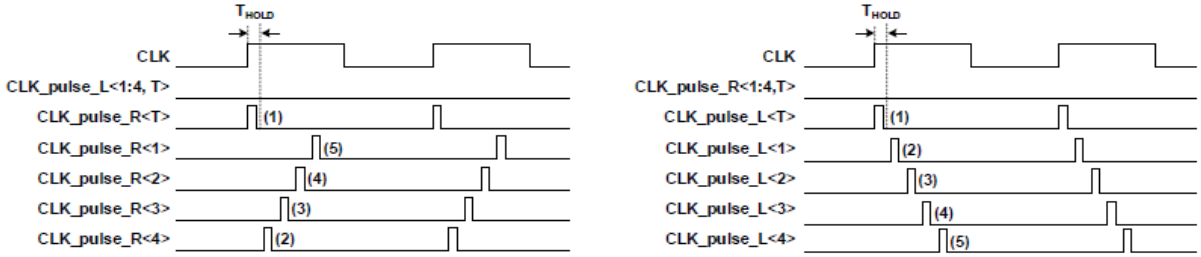

Fig. 3. Waveforms of the pulse generation of bidirectional shift-register when (a)right-shifting & (b)left-shifting

Fig. 3 shows the operation waveforms of the bidirectional shift-register when right-shifting and left-shifting. When right-shifting, CLK_pulse_R<T> first updates the temporary data T0 to the input signal (IN). Simultaneously, in the sub bidirectional shift-register #1, the temporary data T<1> is updated to Q<4>. And then, the latch data Q<4>-Q<2> are

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sequentially updated to their left latch data Q<3>-Q<1>. Finally, the first latch data Q<1> is updated to T<0>, which holds the input signal (IN). Other sub bidirectional shift-registers operate in the same way as the sub bidirectional shift-register #1.

III. PROPOSED DECODER ENABLED BIDIRECTIONAL SHIFT-REGISTER

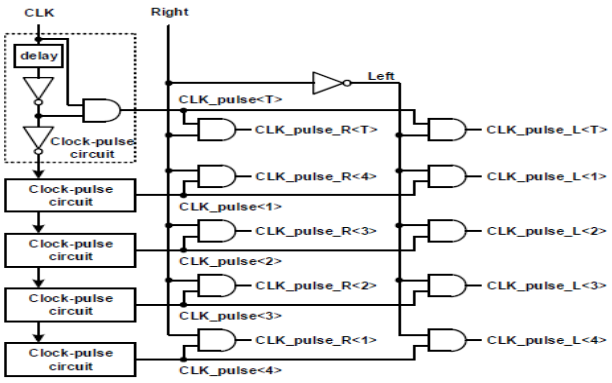

Fig. 4. Proposed bidirectional delayed pulsed clock generator

On the other hand, when left-shifting, the latches except the temporary latches operate in the reverse order of the right-shifting. Therefore, the proposed bidirectional shift-register can shift data to the right or to the left. The proposed bidirectional shift-register stores IN to the temporary latch data T<1> or T<64> at the first pulsed clock signal. It can minimize the hold time (THOLD) of the input signal (IN). The pulsed clock signals are generated by the proposed bidirectional delayed pulsed clock generator in Fig. 4. The delay block is implemented with a 4-inverter chain. In digital electronics, a binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. They are used in a wide variety of applications, including data demultiplexing, seven segment displays, and memory address decoding. There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple data inputs and multiple outputs that converts every unique combination of data input states into a specific combination of output states. In addition to its data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states. Depending on its function, a binary decoder will convert binary information from n input signals to as many as 2^n unique output signals. Some decoders have less than 2^n output lines; in such cases, at least one output pattern will be repeated for different input values. A 1-of-n binary decoder has n output bits, and the integer inputs bits serve as the "address" or bit number of the output bit that is to be activated. This type of decoder asserts exactly one of its n output bits, or none of them, for every unique combination of input bit state. Each output bit becomes active only when a specific, corresponding integer value is applied to the inputs.

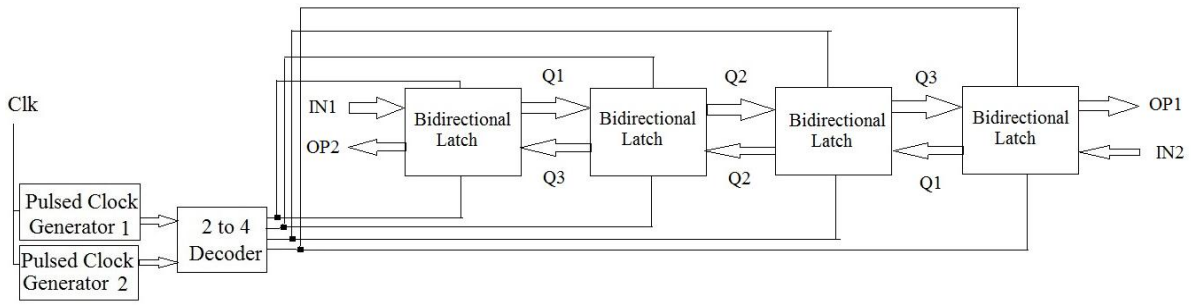

Fig. 5. The proposed bidirectional shift-register

Fig. 5 shows the proposed bidirectional pulsed-latch (BD-PL) based decoder. It reduces the number of pulsed clock generators to half. In order to generate four pulses, the outputs of two pulsed generators are given to 2:4 decoder to generate four pulses. Thus, the overall are is reduced in the proposed method.

IV. EVALUATION RESULTS

Low power and area efficient bi-directional shift register using decoderenabled pulsed latches is proposed. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal.

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A small number of the pulsed clock signals are used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

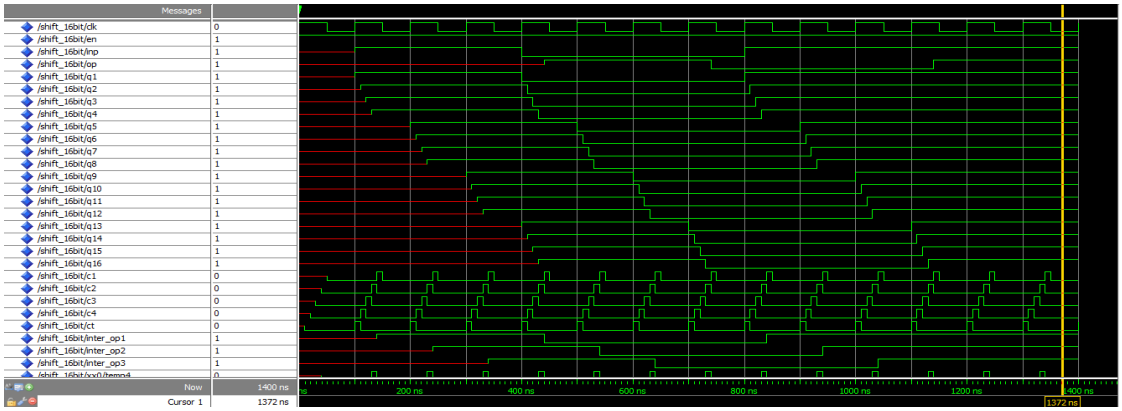

Fig. 6. 16-bit bidirectional shift register based on cascaded pulsed generator

Fig. 6 shows the simulation result of proposed decoder enabled bidirectional shift register. RTL design is done using VHDL and simulated using Modelsim. Table I show that various parameters like area, power and delay of 16 bit existing and proposed bidirectional shift register. RTL design is synthesized using Xilinx ISE and its parameters are compared. As shown in Table I the proposed design produce better results in terms of area and power without any performance degradation.

Table I Comparison Results of Bi-directional Shift Register

Parameters	Area (Gate Count)	Power (mW)	Delay(ns)
Exiting Bidirectional Shift Register	206	168.80	2.451
Decoder Enabled Bidirectional Shift Register	160	150.45	2.451

V. CONCLUSION

Low power and area efficient bi-directional shift register using decoderenabled pulsed latches is proposed. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. The proposed bi-directional shift register saves 22.3% area and 11.2% power compared to the conventional shift register with flip-flops.

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