IJIREEICE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

NCIET- 2020

National Conference on Innovations in Engineering & Technology

Govt., Polytechnic College, Palakkad, Kerala

Vol. 8, Special Issue 1, February 2020

Performance Analysis of 13 Level Multilevel Inverter for PV Application

Ashly George[1], T G Sanishkumar[2]

M. Tech Scholar, Department of Electrical Engineering, Government Engineering College, Idukki, Kerala, India [1]

Associate Professor, Department of Electrical Engineering, Government Engineering College, Idukki, Kerala, India [2]

Abstract: Solar power generation is an emerging trend in renewable sources of electricity. A Photovoltaic (PV) system is a system composes one or more solar panels combined with an inverter, other electrical and mechanical hardware which use energy from the Sun to generate electricity. The inverter proposed in this topology is a 13-level multilevel inverter has two DC sources making it an asymmetric multilevel inverter. The DC output from PV module is tracked to maximum power using a MPPT and conditioned through boost converter. This new configuration of asymmetrical multilevel inverters uses capacitors as the DC links to create the levels for staircase waveforms and makes a reduction in DC sources. Hence making it is possible to generate 13 levels with lower and unequal DC sources (2VDC and 1VDC). 13 level multilevel inverter has two chargeable capacitors and 14 semiconductor switches. The capacitors are self-charging without any extra circuit. Hence the lower number of components makes it to use in wide range of applications. Main attraction of this multilevel inverter is the creation of the negative voltage levels without any additional circuit (such as H-bridge circuit). The implementing system will be validated with MATLAB/ Simulink and hardware.

Keywords: Photo Voltaic (PV), Maximum Power Point Tracking (MPPT), Perturb and Observe (P&O), Boost converter, 13Level Multilevel Inverter.

I. INTRODUCTION

Multilevel Inverters (MLIs) have been providing the reliable and high quality Voltage Source Converters (VSC) to connect the DC power systems to the AC power systems. Multilevel Converters has become an interesting area in the field of industrial applications as it has the ability to work under medium and high power applications. This ability of multilevel inverter against two levels inverters makes them leading converter in photovoltaic systems, HVDC for transmission line, wind turbine, electrical vehicle and power grid etc. One among the main attractions is that MLIs are available in different configurations making them an interesting device in power electronics area. Recently MLIs are used in wide range application in power system because of its availability in different configuration. Advantages of MLIs includes high resolution on the output voltage, low harmonic components because of a high number of output levels, low stress on switches, modularity, and scalability due to cascade connection ability. Different configurations of Multi-level converter are Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascade H-bridge (CHB). Unbalanced DC links and high stress on switches are the disadvantages of NPC and huge capacitors in case of FC. Early mentioned disadvantages had made researchers to focus on CHB with reduced number of components. Some aspects has to be considered like number of levels, the number of DC sources, the number of semiconductors, Total Standing Voltage (TSV), the inherent creating of negative levels and etc.

A DC source can generates one level by two switches and making a module, which can be connected in series to generate more levels. But all the levels generated by these modules are positive levels; hence additional circuits have to be used to generate negative levels. H-bridge is added to the series modules for staircase sinusoidal waveform (negative and positive half-cycles). The semiconductors of H-bridge create negative voltage levels and can tolerate high switching stress. An important issue in the configuration of MLIs is to produce higher output voltage levels using lower components. The above issue can be achieved by apply unequal DC sources. Hence asymmetric multilevel inverters with unequal DC links present a new type of configuration which reduced the number of components along with higher output voltage levels. But stress on switches should be considered due to unequal DC sources. The stress on switches is introduced with Total Standing Voltage (TSV) which is a total highest voltage of each switch in off mood. Evolution of MLIs made reduction in components, especially by replacing DC sources with capacitors. This paper put forward 13 level multilevel inverter with semiconductors, mixed DC sources and capacitors as DC links to achieve maximum voltage levels from DC sources which improves cost and power quality. 13 level multilevel inverter uses two unequal DC sources, 1VDC and 2VDC to generate 13 output voltage levels (6 positive levels, 6 negative levels and a zero level) without DC source with 2VDC charges the capacitor with 2VDC without the use of an additional circuit. Fig.1 & Table 1 shows switching patterns. Polarity of diodes and bidirectional any additional circuit to generate negative voltage levels.

IJIREEICE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
NCIET- 2020
National Conference on Innovations in Engineering & Technology
Govt., Polytechnic College, Palakkad, Kerala
Vol. 8, Special Issue 1, February 2020

II. 13 LEVEL MULTILEVEL INVERTER FOR PV APPLICATION

The block diagram of 13 level inverter for PV application is shown in figure 1.1. The output from the PV panel is taken and is tracked to maximum power and is boosted to required voltage(2VDC) by a boost converter. The output from Boost converter is given as input to 13 level asymmetric multilevel inverter. A DC source supplying 1VDC is given as second input to the 13 level multilevel inverter.

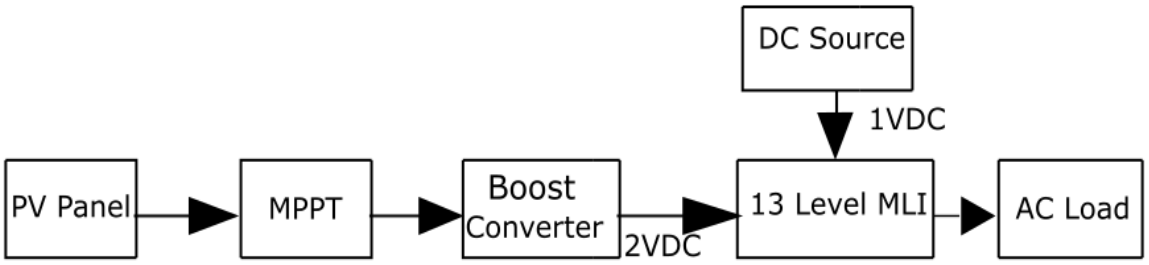

Fig. 1. Block diagram of 13 level multilevel inverter for PV application

13 level multilevel inverter uses two unequal DC sources, 1VDC and 2VDC to generate 13 output voltage levels (6 positive levels, 6 negative levels and zero level) without any additional circuit to generate negative voltage levels. 14 power electronics switches, two capacitors and two unequal DC sources are used in this module. These modules can be cascaded easily to produce higher output voltage levels. In this topology, 1VDC is supplied by DC source and 2VDC is supplied from PV panel. Solar power generation has emerged as one of the most rapidly growing renewable sources of electricity. A photovoltaic (PV) system is a system composed of one or more solar panels combined with an inverter and other electrical and mechanical hardware that use energy from the Sun to generate electricity. The DC output from PV module is tracked to maximum power using a MPPT and is boosted to desirable voltage 2VDC using a boost converter. The output from Boost converter is given as input 2VDC of 13 level asymmetric multilevel inverter. Unequal DC sources
for asymmetric multilevel inverters creates different number of output voltage levels and helps in lowing the harmonics and number of semiconductors. Capacitors make extra DC links hence giving four DC links. Fig 2 shows 13 level multilevel inverter with 14 switches(8 unidirectional switches and 3 bidirectional switches), 14 diodes and 2 unequal DC source and 2 capacitors, generating six positive levels, six negative levels and zero level (13 levels totally). Negative levels are generated without any extra circuit removing H-bridge. The DC source with 1VDC charges the capacitor with 1VDC, and
onal switches suppress the switches hence assuring no short- circuit occur. Table 1 indicates switch modes in each level. Switch (S1, S7), (S3, S8) and (S5, S9) are not turned on at the same time to prevent the short circuit between the two DC sources.

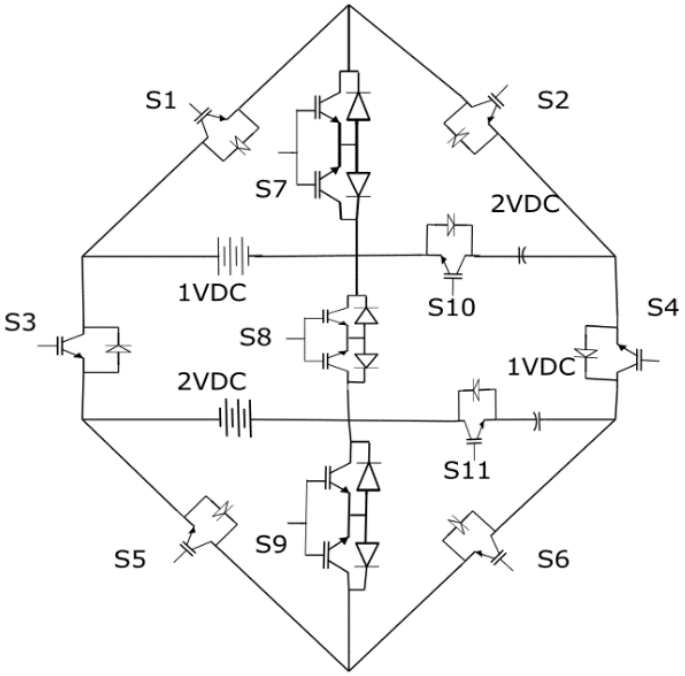

Fig. 2. 13 level multilevel inverter

IJIREEICE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
NCIET- 2020
National Conference on Innovations in Engineering & Technology
Govt., Polytechnic College, Palakkad, Kerala
Vol. 8, Special Issue 1, February 2020

Number of switches turned on per one cycle for each switch is shown in Table I.

	Based on number of module units	Based on number of desired levels
Level	12n+1	N_L
Number of Switches	14n	$14\left[\frac{N_L-2}{12}+1\right]$
Number of Diodes	14n	$14\left[\frac{N_L-2}{12}+1\right]$
Driver	9n	$11\left[\frac{N_L-2}{12}+1\right]$
DC Sources	2n	$2\left[\frac{N_L-2}{12}+1\right]$
Capacitors	2n	$2\left[\frac{N_L-2}{12}+1\right]$
TSV	32n	$32\left[\frac{N_L-2}{12}+1\right]$

Table I The equations of 13 level multilevel inverter

Fig.3 shows schematic output voltage of the inverter. It is notable from Fig.3 that switches S2, S3, S4 and S8 are turned on at low frequency, which is to reduce the switching losses. Fig.3 also shows how DC sources and capacitors are employed for each level.

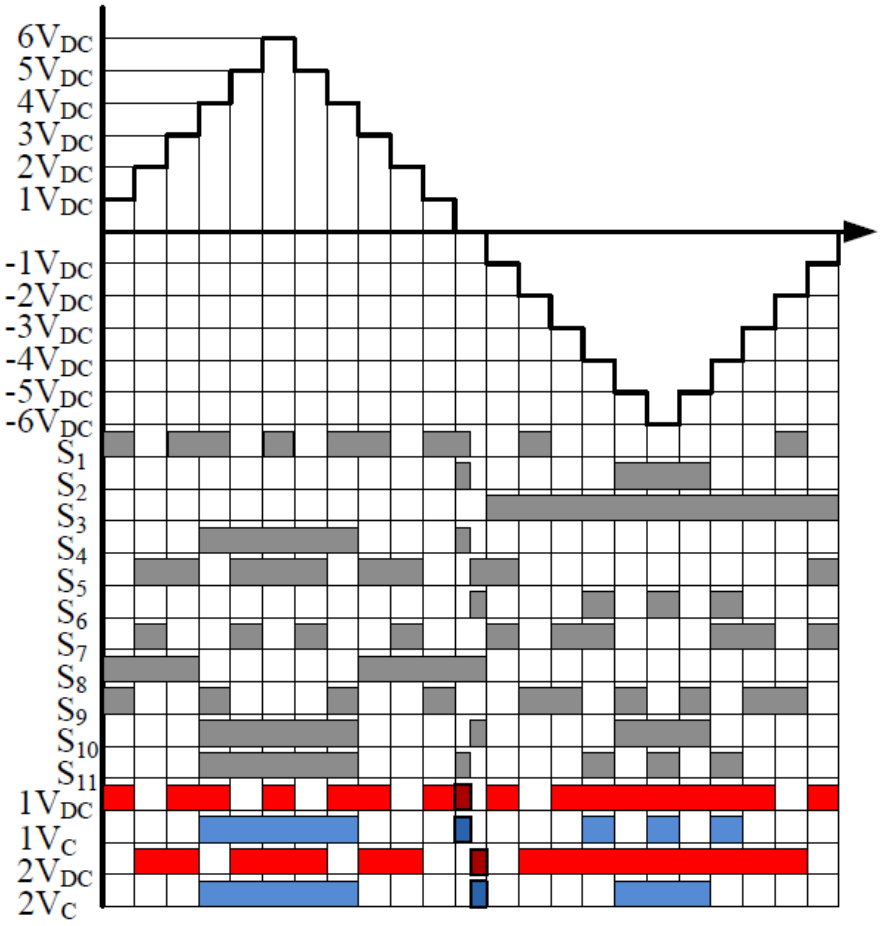

Fig. 3. Switching pattern of 13 level multilevel inverter(one cycle)

Capacitors as a DC links are used in levels 4th, 5th and 6th. Main feature of this inverter is the charging of capacitors without any additional circuit. Capacitors have been charged in level zero. DC source with 1VDC is charging 1Vc and DC source with 2VDC

IJIREEICE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
NCIET- 2020
National Conference on Innovations in Engineering & Technology
Govt., Polytechnic College, Palakkad, Kerala
Vol. 8, Special Issue 1, February 2020

is charging 2Vc. The discharging of capacitors is in some levels of one cycle and also mixed DC sources and capacitors as the DC links cause the smooth behaviour of capacitors. The equations of the module are shown in Table 2 showing the number of the semiconductor, DC sources, capacitors and drivers based on the number of module units (n) and the number of output levels (NL). TSV (Total Standing Voltages) of the circuit is shown in Table II which is the sum of all blocking voltages for the switches.

III. SIMULATION RESULT

A 13 level multilevel inverter for PV application is shown through simulation with two different DC source, 1VDC=10V, 2VDC=20V (20V is supplied from PV Panel)

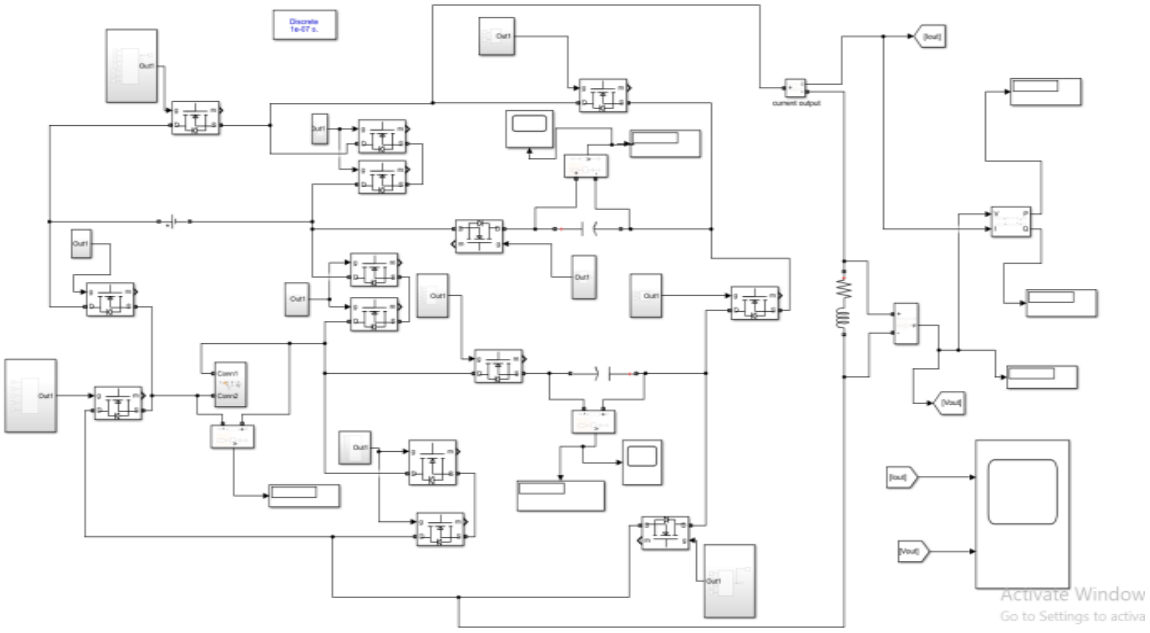

Fig. 4. 13 Level multilevel inverter for PV application

Below shows the waveform of output voltage and current of 13 level multilevel inverter for PV application, fig.5 1VDC and 2VDC supplied from a DC source and fig.6 IVDC supplied by DC source and 2VDC supplied from PV panel. As mentioned in the paper no additional circuit is needed to create both positive and negative levels, generation of negative level is made possible because of the unequal source 1VDC and 2BDC.Through FFT analysis the THD% obtained is 5.95% in simulation, this value will further reduce when analysis is done on the hardware. Cascading can increase the output voltage levels. through cascading 25 levels (12 positive levels, 12 negative levels and zero level) and 169 levels (84 positive levels, 84 negative levels and zero level) can be generated. Other advantage is harmonics will be reduced i.e low THD value.

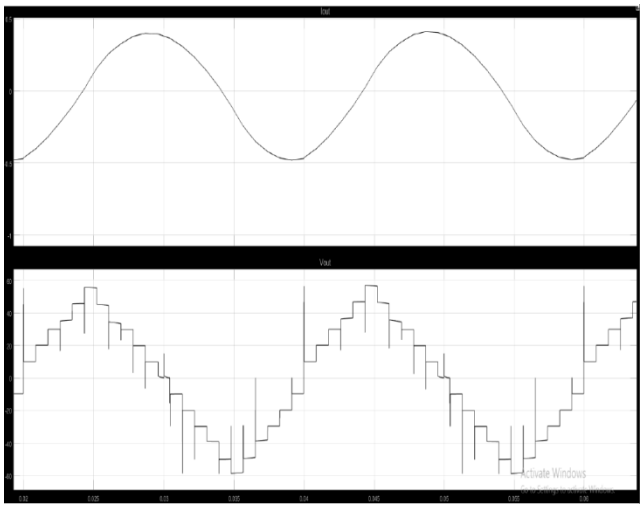

Fig. 5. 13 level multilevel inverter with 1VDC=10V, 2VDC=20V.

IJIREEICE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

NCIET- 2020

National Conference on Innovations in Engineering & Technology

Govt., Polytechnic College, Palakkad, Kerala

Vol. 8, Special Issue 1, February 2020

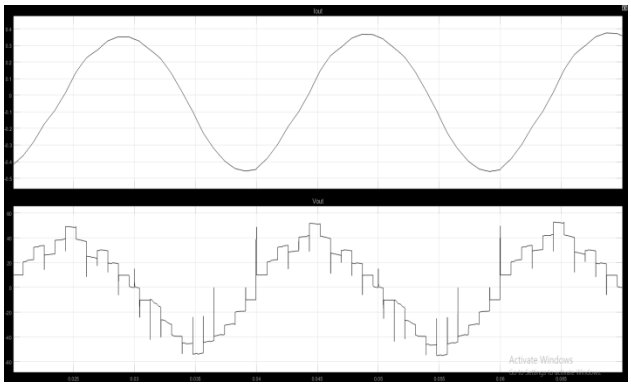

Fig. 6. 13 level multi inverter with 1VDC=10V, 2VDC from PV panel

IV. CONCLUSION

This paper introduces a new topology for asymmetrical multilevel inverter to produce 13 levels by two DC sources for PV application. The 13 level multilevel inverters named K-Type as it looks similar to kite. K-type provides two extra DC links with the use of capacitors to generate more output levels and to create staircase waveform. Lower number of components are used such as two DC sources, two capacitors,14 semiconductor switches. this inverter can be used in power applications with unequal DC sources with ratio 1:2. Main feature is its modularity modularized different strategies in cascade arrangements to create high voltage outputs with low stress on semiconductors and lower number of devices. This ability can be utilised in some special applications such as solar farm along with a lot of DC sources, with different voltage amplitudes. The other advantage of K-Type inverter is its capability to generate both positive and negative output voltage without any additional circuit. THD% obtained is 5.95% in simulation. Completed simulation is shown in above simulation result.

REFERENCES

[1]. Babaei, E. Kangarlu, M.F. ; Sabahi, M. Extended multilevel converters: attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters IET Power Electronics, Volume 7, level 1, January 2014, p. 157 166.
[2]. A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)', Power Electronics, IEEE Transactions on, 2015, 30(1), 450-462.
[3]. E.Samadaei, M.Kaviani, K.Bertilsson, A 13-levels Module(K-Type) with 2 DC sources for Multilevel Inverters, IEEE Transactions on Industrial Electronics.
[4]. A. Taghvaie, J. Adabi and M. Rezanejad, "A Multilevel Inverter Structure Based on a Combination of Switched-Capacitors and DC Sources," in IEEE Transactions on Industrial Informatics, vol. 13, no. 5, pp. 2162-2171, Oct. 2017
[5]. Rasoul Shalchi Alishah ; Daryoosh Nazarpour ; Seyyed Hossein Hosseini ; Mehran Sabahi. "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels" IET Power Electronics, Volume 7, Issue 1, January 2014, p. 96 – 104.
[6]. X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du and Z. Lu, "A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques," in IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 7184-7194, Nov. 2016.
[7]. E. Samadaei, S. A. Gholamian, A. Sheikholeslami and J. Adabi, "An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters With Reduced Components," in IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 7148-7156, Nov. 2016.
[8]. E. Samadaei, A. Sheikholeslami, S. A. Gholamian and J. Adabi, "A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters," in IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 987-996, Feb. 2018.