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ECG Processor with Optimised Hybrid Classifier for Cardiovascular Arrhythmia

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Abstract: This paper presents the design of an energy-efficient Electrocardiogram (ECG) processor for arrhythmia detection and classification of life-threatening arrhythmia plays an important part in dealing with various cardiac conditions. It provides better time and frequency resolution of the Electrocardiogram (ECG) signal, which helps in decoding important information of an ECG, which improves the arrhythmia classification. The decisions can be achieved by determining different intervals such as PR Interval, RR Interval, Heart Rate etc. and those intervals will be compared with the ideal intervals. During the whole process Modelsim was used & ECG signals were taken from PhysioBank ATM. The proposed QRS detection architecture deals with almost all the ECG signal artifacts, such as low-frequency noise, baseline drift, and high-frequency interference with minimum hardware resources. Few metrics needed to be concerned during the implementation of ECG processor are Accuracy (low detection error-rate), Area (hardware resource utilization), Power efficiency (low power consumption), Speed (delay), Sensitivity (real time monitoring) And Predictivity. Thereby, in this proposed project we are going to simulate the results and compare few performance metrics with the existing methodology.

Keywords: Electrocardiogram, QRS complex, hybrid classifier, multi-scaled product, soft-threshold algorithm, wavelet ECG detector.

I. INTRODUCTION

Cardiovascular arrhythmia is a very common disease that might cause sudden death in some cases if it is not treated in time. there are various types of arrhythmias such as Atrial fibrillation, Atrial flutter , Supraventricular Tachycardia (SVT), Ventricular tachycardia, Ventricular fibrillation, Long QT syndrome ,etc. and each type is associated with a pattern, as such the P wave, which represents the depolarization of the atria; the QRS complex, which represents the depolarization of the ventricles; the T wave, which represents the repolarization of the ventricles; and The U wave represents papillary muscle repolarization. Normal rhythm produces four entities – a P wave, a QRS complex, a T wave, and a U wave – that each has a fairly unique pattern. The arrhythmias can be classified into two major categories. The first category consists of arrhythmias formed by a single irregular heartbeat, herein called morphological arrhythmia. The other category consists of arrhythmias formed by a set of irregular heartbeats, herein called rhythmic arrhythmias. The classification of normal heartbeats and the ones composing the former group are on the focus of this survey. These heartbeats produce alterations in the morphology or wave frequency, and all of these alterations can be identified by the ECG exam. The process of identifying and classifying arrhythmias can be very troublesome for a human being because sometimes it is necessary to analyze each heartbeat of the ECG records, acquired by a holter monitor for instance, during hours, or even days. In addition, there is the possibility of human error during the ECG records analysis, due to fatigue. An alternative is to use computational techniques for automatic classification.

In recent years, with the development in algorithms for automatic heartbeat classification, some ECG processors integrating machine learning accelerator have been proposed to provide on-chip cardiac disease diagnosis. Thereby cpu assisted processing requires high processing frequency and leads to a large power consumption. Consequently, implementing algorithmic and architectural level approaches improving energy efficiency while retaining high accuracy is a big challenge for ECG diagnosis processor.

This paper proposes a full automatic system for arrhythmia classification from signals acquired by an ECG device can be divided as follows: (1) ECG signal preprocessing; (2) heartbeat segmentation; (3) feature extraction; and (4) classification. In each of the four steps, an action is taken and the final objective is the discrimination/identification of the type of heartbeat. In this proposed process, band pass filter was used to reduce the noise of the signal. In order to achieve high detection accuracy with low power consumption, a soft-threshold algorithm is used in our ECG detector with its efficient hardware implementations. The hybrid classifier that includes a Weak Linear Classifier (WLC) and a

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strong Support Vector Machine (SVM) classifier. WLC can only identify the beats with distinct characteristics by performing simple threshold comparisons based on beat interval feature and a novel morphology feature named QRS area ratio. The beats that are unclassified by WLC will activate the more powerful but energy-guzzling SVM classifier. The overall accuracy and power consumption features of the design when compared to a single classifier are improved in this proposed electrocardiogram processor. The paper is organized as follows section II existing methodology, section III proposed methodology and section IV result and discussion.

II. EXISTING METHODOLGY

2.1 ECG Signal Preprocessing

This existing ECG detector is based on wavelet transforms and it was applied to reduce noise and baseline variation of the ECG signal. Since they preserve ECG signal properties avoiding loss of its important physiological details and are simple from a computational point of view.

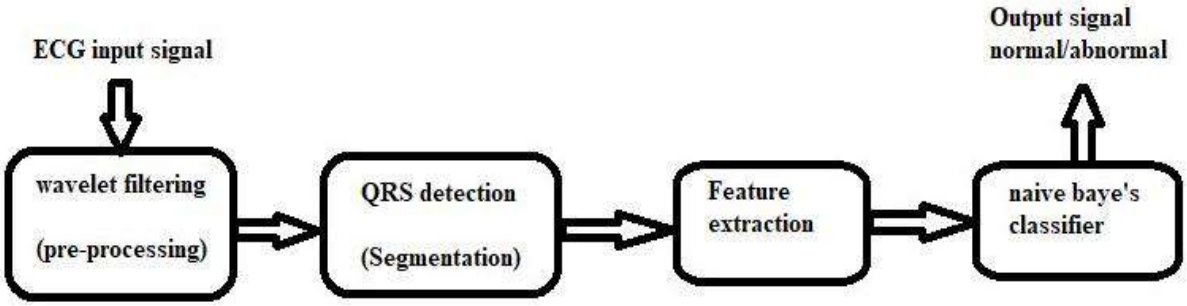

Figure 1 Flow chart of the existing system

2.1.1 Wavelet Decomposer:

The wavelet ECG detector consists of Wavelet Filter Banks (WFBs) as a wavelet decomposer, a Generalized Likelihood Ratio Test (GLRT), with the threshold function as a QRS complex detector and a noise detector with zero crossing points. First, the WFBs decompose the input ECG signals into sub-bands with two monophasic and biphasic outputs. The GLRT with threshold function estimates the heart-beating rate with the decomposed WFB outputs. The noise detector reduces the power consumption by determining the operation mode according to the SNR of the ECG input signal.

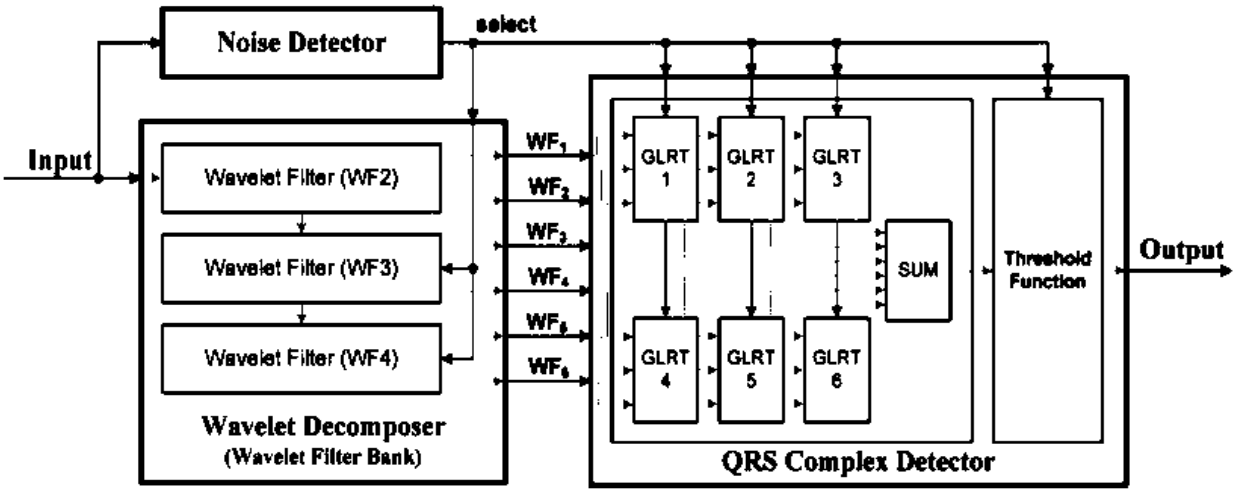

Figure 2 Block diagram of conventional wavelet ECG detector

To implement wavelet transformer, both the decimator (down sampler) based and undecimator based architectures with the filter pairs of Low-Pass Filter (LPF) and High-Pass Filter (HPF) have been used. The undecimator based architecture has the advantage of translation-invariance but requires a constant clock and many registers.

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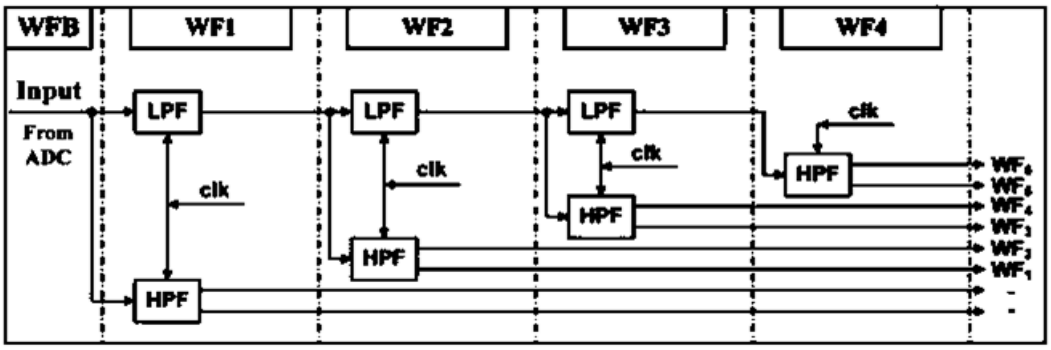

Figure 3 Undecimator based wavelet filter bank

Here, and are the transfer functions of LPF and HPF, respectively, in the WFBs which are shown in Figure. As a result, since the wavelet decomposer can be simplified to several add and shift operations, the number of required logic gates is significantly reduced, thus lowering the power consumption and area.

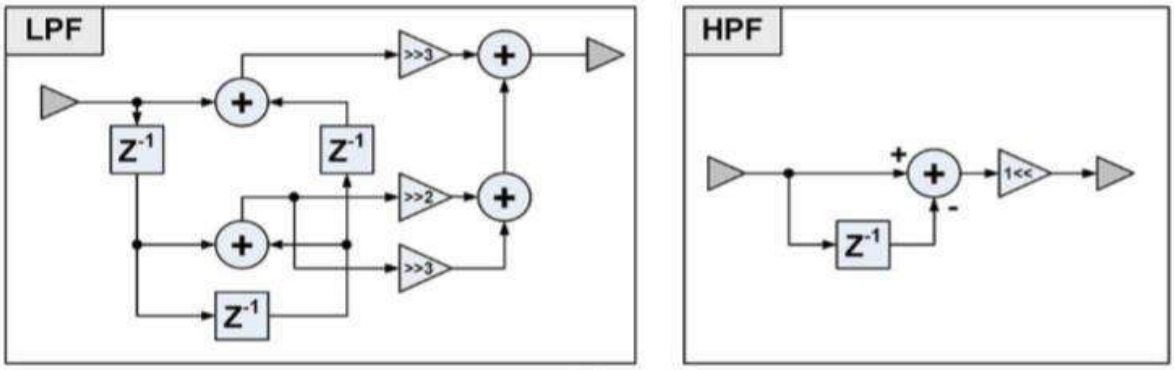

Figure 4 Schematic diagrams of low-pass and high-pass filter in wavelet filter bank

2.1.2 Noise Detector

The noise level inside the ECG detector is measured by counting the number of zero-crossing points in a certain time interval.

2.2 QRS Complex Detector

The wavelet QRS complex detector uses the hypothesis testing of the GLRT. Since the GLRT uses the maximum - likelihood estimation of unknown parameters, the implementation of each GLRT block requires a considerable number of registers, adders and multipliers as shown in Figure. The GLRT determines the presence of R waves according to the test computations expressed as $\mathbf{T(n) = X(n)^T H (H^T H)^{-1} H^T X(n),}$ where x(n) is the input to the WFB and H is the linear combination matrix of representative functions.

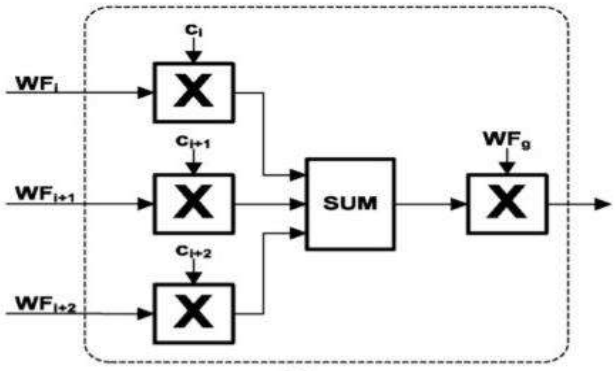

Figure 5 Schematic diagram of GLRT block

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2.3 Feature Extraction

The feature extraction stage is the key to the success in the heartbeat classification of the arrhythmia using the ECG signal. Any information extracted from the heartbeat used to discriminate its type maybe considered as a feature. Features extracted from the domain of time/frequency together with the features of the RR interval appear as part of the methods that produced the highest accuracies in literature to date. The simplest way to extract features in the time domain is to utilize the points of the segmented ECG curve, i.e., the heartbeat, as features.

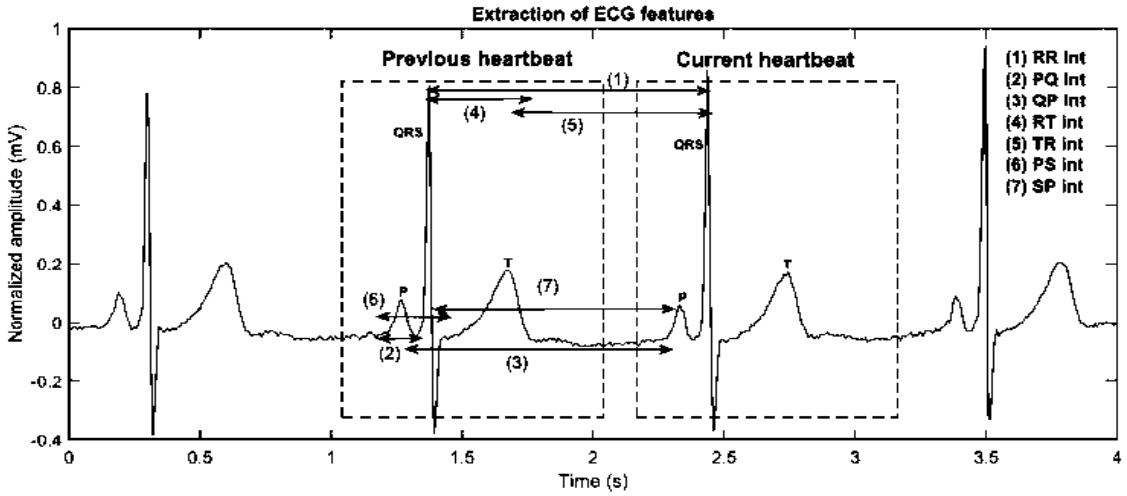

Figure 6 ECG feature extraction from two consecutive heartbeats.

2.4 Naive Bayes Classifier

The naive Bayes classifier is easy to build with no complicated iterative parameter estimation, which makes it particularly useful for hardware implementation. It assumes naive and strong independent distributions between the feature vectors, and this assumption was met, since all the extracted ECG features were independently analyzed and assessed from the beginning. The training data are stored in an off-chip memory because of its size.

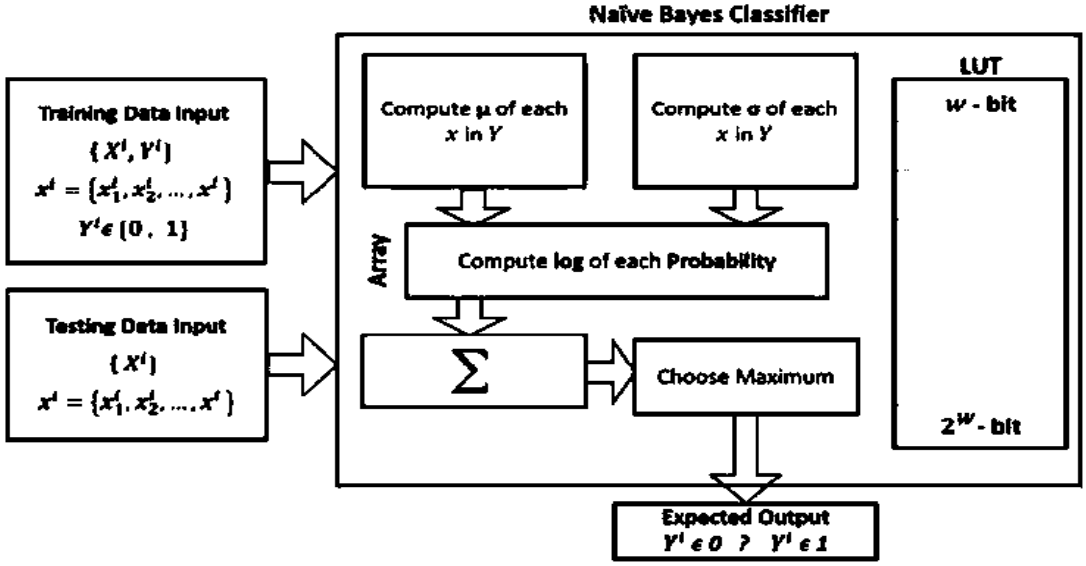

Figure 7 Architecture of naive bayes classifier

2.5 Conclusion of The Performance of Existing System

In order to achieve low power with high detection rate, the proposed QRS complex detector in our ECG detector is based on naive Bayes classifier. ECG detector with the front-end SAR-ADC with the on/off time-controlled comparator and passive S/H is implemented using0.35 CMOS technology. The active die area occupies 2.81 and the test chip shows a low detection error-rate of 0.196% and low power consumption of 19.02 at 3 V supply voltage.

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III. PROPOSED SYSTEM

The proposed system consists of four main stages, which are the ECG preprocessing, segmentation, feature extraction, and classification. New techniques are presented in this stage to increase the robustness of the system, and this is by utilizing adaptive search windows and thresholds to accurately detect the fiducial points in each heartbeat.

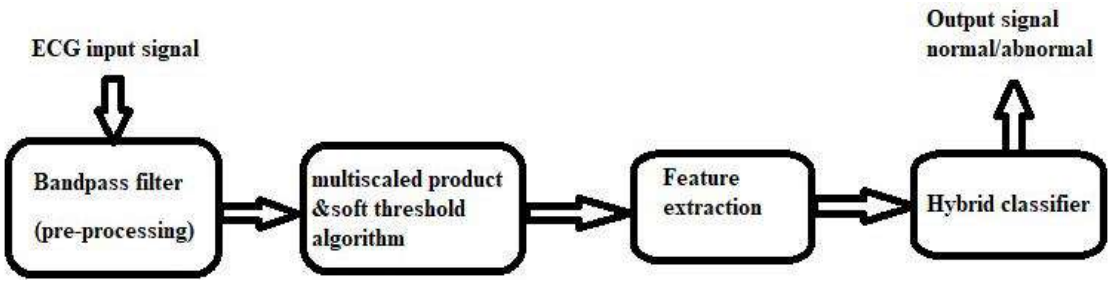

Figure 8 Flowchart of the proposed model

3.1 Pre-processing

In the first stage, the ECG preprocessing is responsible for following tasks: 1) ECG filtering; 2) QRS complex detection;

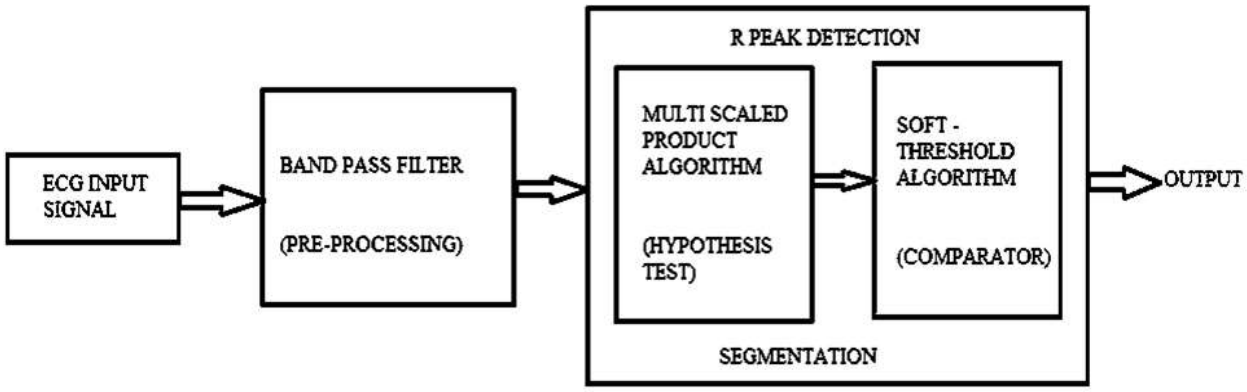

Figure 9 Block diagram of ECG preprocessing stage

3.1.1 ECG Filtering The filtering of the ECG signal was done through a cascaded LPF and HPF. Band-pass filtering of the raw ECG signal is the first step in which the filter isolates the predominant QRS energy centered at 10 Hz, and attenuates the low frequencies characteristic of the P and T waves, baseline drift, and higher frequencies associated with electromyographic noise and power line interference. The main important point is not to lose the information carried by the ECG signal after being filtered out. The two filters have shown a good performance in cleaning up the ECG signal from the coupled noise. The difference equations of the cascaded LPF and high-pass filter (HPF) are given in (1) and (2), respectively.

$$y(nT) = 2y(nT - T) - y(nT - 2T) + x(nT) - 2x(nT - 6T) + x(nT - 12T) \quad (1)$$

$$y[nT] = x(nT - 16T) - \frac{1}{32}[y(nT - T) + x(nT) - x(nT - 32T)]. \quad (2)$$

The cut-off frequency of the LPF filter is 11 Hz, and it introduces a delay of six samples, whereas the HPF has a cut-off frequency and delay of 5 Hz and 16 samples, respectively. The coefficients of the filters are all integers and of power-of-two, which make them suitable for hardware implementation.

3.1.2 Multi-Scaled Product Algorithm and Soft Threshold Algorithm

In our multi-scaled product block, only 1 multiplier and 2 multiplexers are only needed. Due to the reduced number of multiplication operations, its hardware complexity and power consumption are significantly lower. However, especially under low SNR condition, the output can sometimes have a peak signal when the magnitude of the T point signal in the ECG signal is sufficiently high, which results in duplicated detections.

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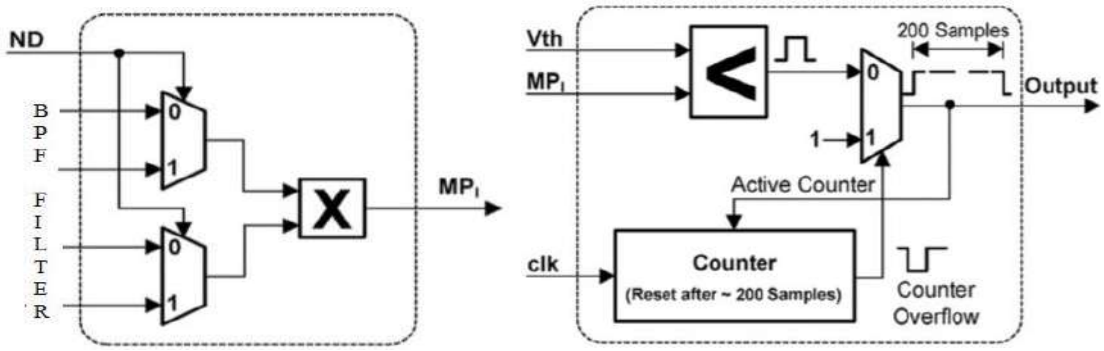

Figure 10 Architecture of multi-scaled product algorithm and soft threshold algorithm.

To boost the QRS detection accuracy, we used a soft-threshold algorithm, which can be implemented without large power and area overheads. Consequently, the combination of the multi-scaled product and soft-threshold algorithm and its efficient hardware implementations leads to a low power and highly reliable QRS detector. In order to remove the failure occurred in the QRS complex detection, the soft-threshold algorithm, which uses variable thresholds rather than a hard threshold, is presented. With the known minimum RR interval of 200 mS or less which is limited by the depolarization of atria and ventricles, the adoption of a soft threshold can remove the error by T point signal. When the comparator detects the QRS complex at which the output of the comparator goes to high, the threshold is changed to a higher value. The changed threshold is kept while 200 samples pass over the T point signal. If T-wave comes after 200 mS, our detector may make a false detection.

3.2 RR Interval Features Extraction Stage

R is a point corresponding to the highest peak of the ECG waveform, and RR interval is the time between the successive QRS complexes. The ECG signal has a nonlinear dynamic behaviour, and during arrhythmia, nonlinear dynamic components change more significantly than the linear counterparts. RR interval is simple, easy to calculate, and less prone to noise.

3.3 Hybrid Classifier

The hybrid classifier includes a low complexity WLC and a non-linear SVM classifier. PCA is employed for feature dimension reduction to reduce the complexity of SVM for classification. WLC aims at filtering out the beats with obvious characteristics that can be easily recognized. Only the beats that are unclassified in WLC will be handled by the more computational complicated SVM classifier. As the ratio of beats that can be processed by WLC is a key metrics, an optimized feature set is exploited to enhance the performance. Besides, a simple but effective decision rule for classification is applied with small resource overhead.

3.3.1 Weak Linear Classifier

Since arrhythmia beats are accompanied with short PRIs or large QARs, a configurable WLC is put forward based on these features. The decision rule for classification is listed in equation

$$type = \begin{cases} \mathbf{A} & A_{en} \,\&\, (QAR > A_{QAR}) \,\&\, (PRI < A_{PRI}) \\ \mathbf{N} & (PRI > N_{PRI}) \,\|\, N_{en} \,\&\, (QAR < N_{QAR}) \\ \mathbf{U} & otherwise \end{cases}$$

Where AQAR and APRI are the boundaries for arrhythmia beats based on the features of QAR and PRI. NQAR and NPRI are the corresponding boundaries for normal beats. Aen signifies whether the current judging condition for arrhythmia beats is enabled and Nen indicates whether the QAR based judging condition for normal beats is valid. A and N represent arrhythmia and normal beats respectively. U denotes the beat is unclassified under the decision of WLC and will be further analysed by the SVM classifier. The parameters of AQAR, APRI, NQAR and NPRI are derived based on individual's characteristic and they are set as the mean values of the estimated features from the training dataset. WLC can handle over 40% of the beats and achieves an average filtering ratio of 62.3%.

3.3.2 Support Vector Machine Classifier

SVM is known as an excellent tool for classification and we apply the non-linear SVM with an RBF-kernel as the strong part of the weak-strong hybrid classifier. The SVM classifier is allocated with large resource overhead to identify those beats with ambiguous characteristics, which gains superior performance but also high power consumption. Based on the

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WLC-SVM architecture, the SVM and its related modules such as PCA can be deactivated when WLC alone is sufficient to complete the classification. Besides clock gating technique, retention technique is applied to the large memory in PCA and SVM, which saves about 70% leakage power of the SRAMs when SVM is not active. Since operating frequency is rather low for ECG based wearable systems and static power dominates the total power consumption, the static power saving in the SRAMs contributes a great deal to the total power reduction.

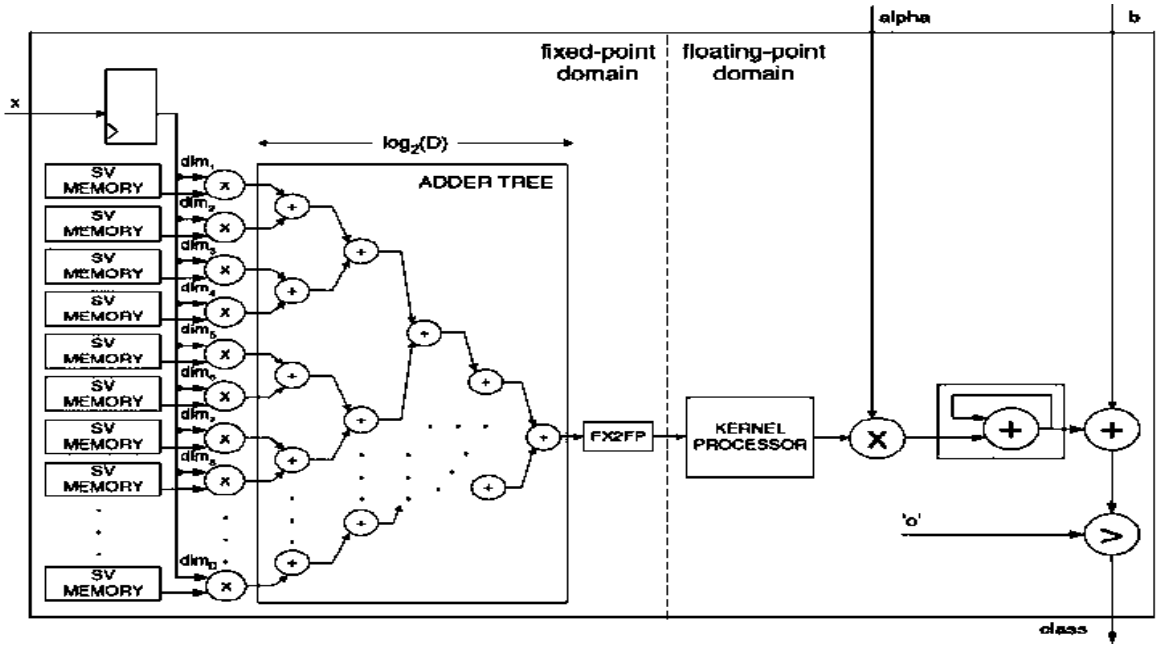

Figure 11 Architecture of support vector machine

With the proposed WLC-SVM classifier and memory retention technique applied to the SRAM, the average leakage energy dissipation of the processor is 537.5uj/beat. The processor with WLC-SVM architecture can achieve 41.7% total energy saving.

IV. RESULT AND DISCUSSION

4.1 Simulation Results

VLSI simulation results resulting in the following advantages Reduces the size of circuits, Reduces cost of the devices, Increases operating speed of circuits, less power consumption. Recently, due to the remarkable advancement in technology, the development of dedicated hardware for accurate ECG analysis and classification in real time has become possible.

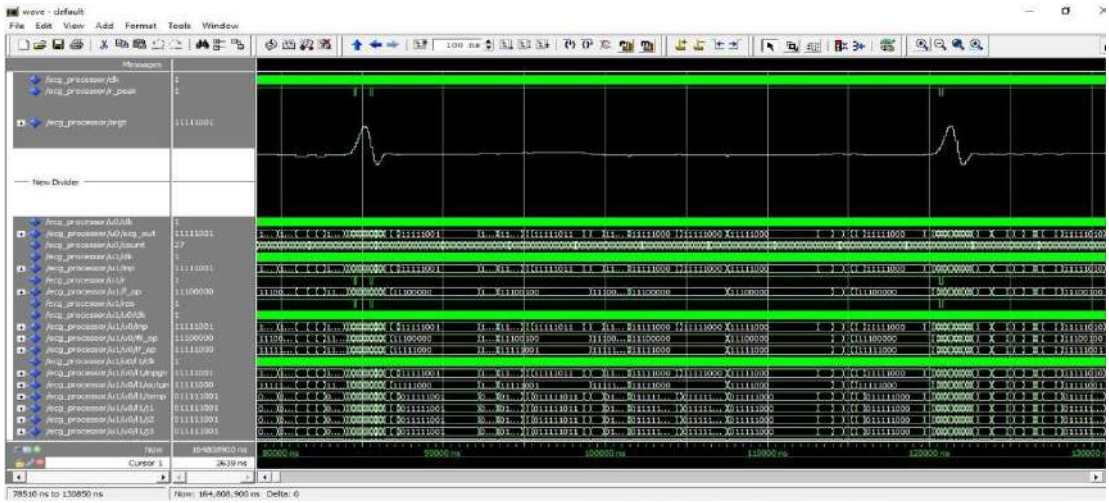

Figure 12 Simulation output detection: R peak for given ECG signal samples.

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The main requirements are low-power consumption and low-energy operation. To test our program, we have used data files taken from PhysioBank ATM of MIT-BIH database. Decision making rules were made taking help from several cardiologists. Five-step procedure was taken to find the arrhythmia. The results shown here gives an easy way to detect different arrhythmias. To improve the accuracy, we need to increase the number of parameters in the decision making process. That will help us to improve the accuracy maintaining the simplicity. Simulator Tools: Xilinx ISE 8.1i AND Model Sim SE 6.3f

This simulation is run based on band pass filter and soft threshold algorithm used in this proposed system.

4.2 Comparison of ECG Detectors

In terms of area, power and delay, proposed ECG detector performance is compared with the previous wavelet based ecg detector.

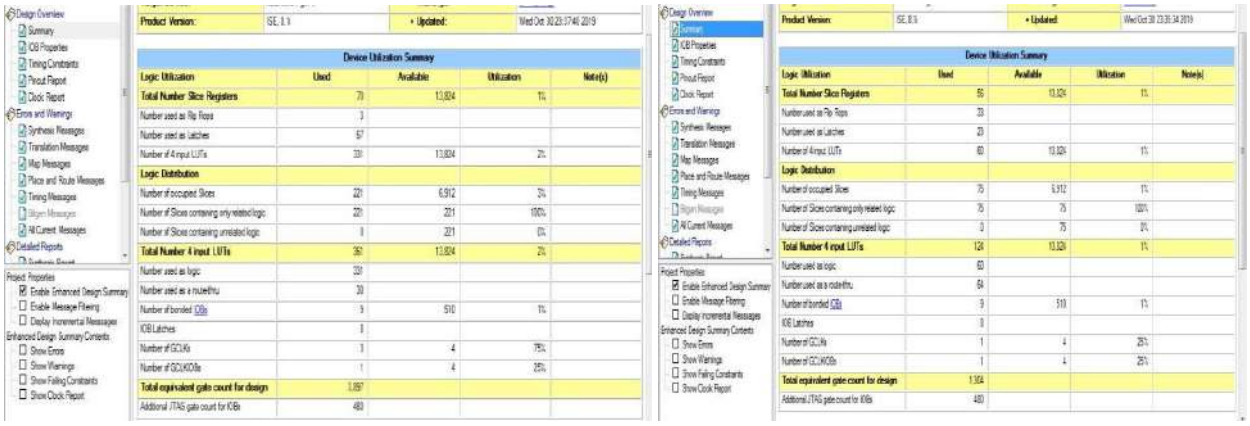

Figure 13 Existing and proposed ECG detector's measured area based on ECG signal filtering and R peak detection

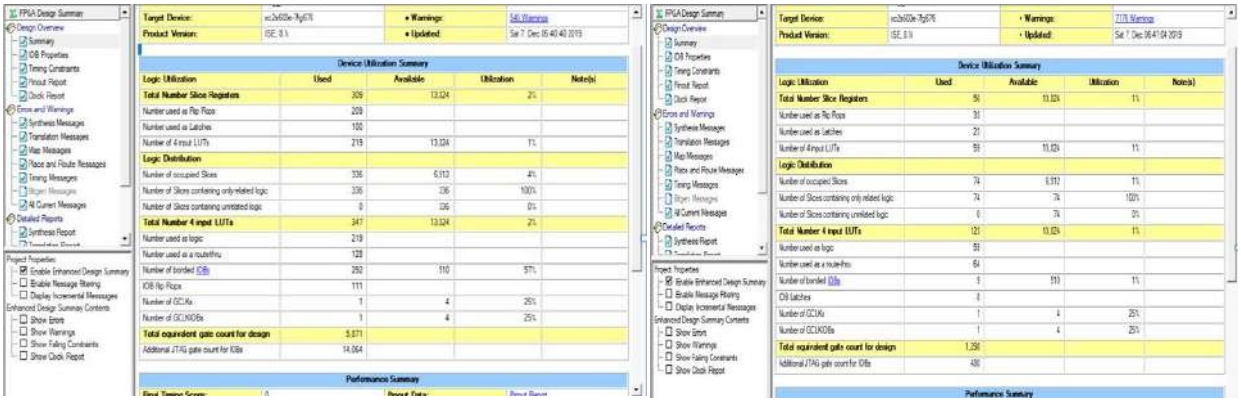

Figure 14 Existing and proposed ECG detector's measured area based on naive baye's classifier and hybrid classifier.

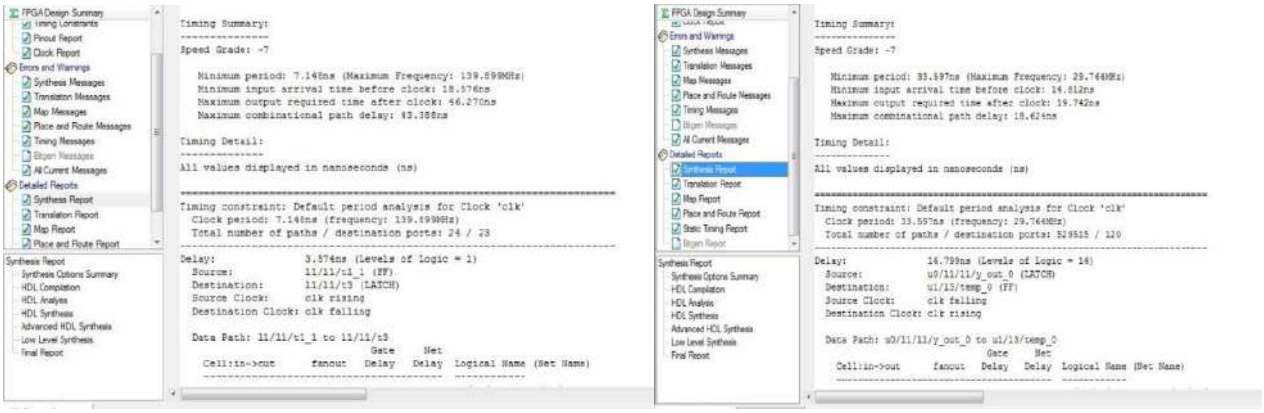

Figure 15 Existing and proposed ECG detector's delay based on ECG signal filtering and R peak detection

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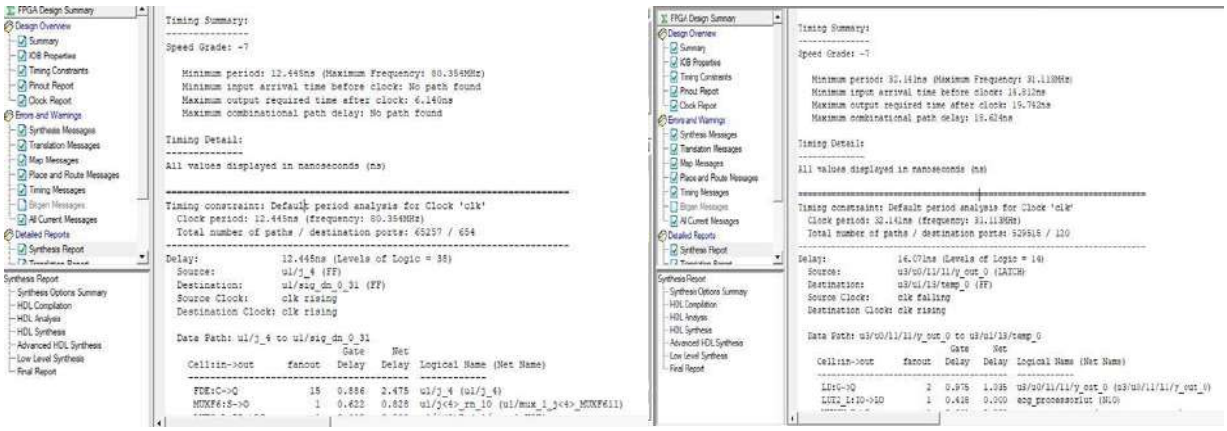

Figure 16 Existing & proposed ECG detector's delay based on naive baye's classifier and hybrid classifier respectively.

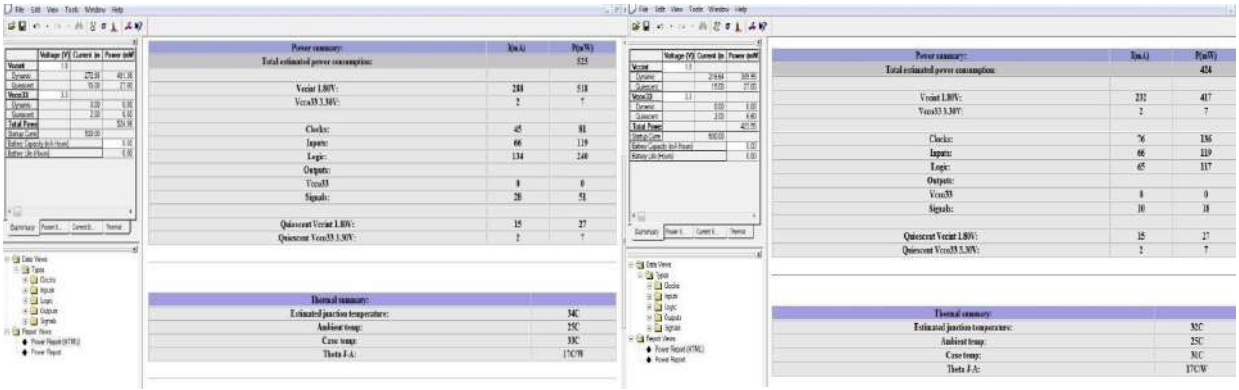

Figure 17 Existing and proposed ECG detector's power consumption based on ECG signal filtering & R peak detection

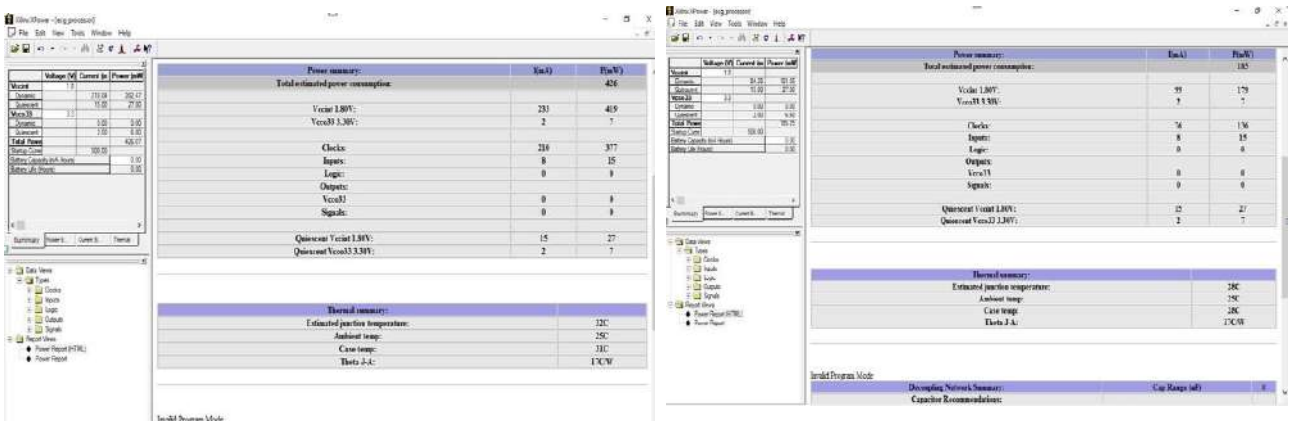

Figure 18 Existing and proposed ECG detector's power consumption based on naive baye's classifier and hybrid classifier respectively.

Table 1 Comparison of area, delay and power of simulated models of ECG detectors

Model	Existing ECG detector	Proposed ECG detector
Total number slice register	305	56
Look up tables	347	123
Equivalent gate count of proposed work	5,871	1,298
Minimum period	12.445ns	32.141ns
Maximum frequency	80.354MHz	31.113MHz
Maximum combinational path delay	1 ns	18.624ns
Total estimated power consumed	419 mW	179 mW

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4.3 CONCLUSION AND FUTURE WORK:

In this paper, the design of an energy-efficient arrhythmia detection processor with hybrid classifier is proposed. The ECG filtering removes the noise coupled with the ECG signal. The processing of the data is done using fixed point representation. The digitized ECG data are applied in series at the input to the preprocessing stage with a resolution of 8 bit, while a variable number of bits were utilized in the different stages to enhance the accuracy and avoid truncations errors. The QRS complex is techniques are presented to increase the robustness of the system and thresholds to accurately detect the fiducial points in each heartbeat. Thus, the proposed QRS complex detector in our ECG detector based on the multi-scaled product algorithm and a soft-threshold algorithm is implemented In order to achieve low power with high detection rate.

Future enhancement can be done by Implementing a less complex strong support vector machine (svm) classifier and Improving the delay to detect the r peak. Further, we can introduce this proposed system in implantable peacemaker as well in the field of network –on –chip.

Applications

- Portable ECG detector
- Wearable arrthymia detector
- Small monitoring ECG processor in clinic

Advantages

- Small equipment
- Low cost device
- Portable

REFERENCES

[1]. Zhijian Chen, Jiahui Luo, Kaiwen Lin, Jiaquan Wu, Taotao Zhu, Xiaoyan Xiang, and Jianyi Meng, “An Energy-Efficient ECG Processor with Weak-Strong Hybrid Classifier for Arrhythmia Detection.” IEEE Trans. Biomed. Eng., vol. 50, no. 8, pp. 999–1001, Aug. 2018.
[2]. Young-Jae Min, Hoon-Ki Kim, Yu-Ri Kang, Gil-Su Kim, Jongsun Park, and Soo-Won Kim,” Design of Wavelet-Based ECG Detector for Implantable Cardiac Pacemakers “, IEEE TRANS. On Biomedical Circuits And Systems, vol.7, no.4,august2013
[3]. Temesghen Tekeste, Hani Saleh, Baker Mohammad and Mohammed Ismail, “Ultra-Low Power QRS Detection and ECG Compression Architecture for IoT Healthcare Devices”, 1549-8328 © 2018 IEEE transactions on circuits and systems.
[4]. Nourhan Bayasi, Temesghen Tekeste, Hani Saleh, Baker Mohammad, Ahsan Khandoker and Mohammed Ismail, “Low-Power ECGBased Processor for Predicting Ventricular Arrhythmia” IEEE Trans. Biomed. Eng., vol. 50, no. 8, pp. 999–1001, Sep. 2003.
[5]. P. S. Hamilton and W. J. Tompkins, “Quantitative investigation of QRS detection rules using the MIT/BIH arrhythmia database,” IEEE Trans. Biomed. Eng., vol. BME-33, no. 12, pp. 1157–1165, Dec. 1986.
[6]. P. de Chazal and R. B. Reilly, “A patient-adapting heartbeat classifier using ECG morphology and heartbeat interval features,” IEEE Transactions on Biomedical Engineering, vol. 53, no. 12, pp. 2535–2543, 2006.
[7]. N.Alajlan,Y.Bazi,F.Melgani,S.Malek,andM.A.Bencherif, “Detection of premature ventricular contraction arrhythmias in electrocardiogram signals with kernel methods,” Signal, Image and Video Processing, vol. 8, no. 5, pp. 931–942, 2014.
[8]. Rabee and I. Barhumi, “ECG signal classification using support vector machine based on wavelet multiresolution analysis,” in Proceedings of 11th International Conference on Information Science, Signal Processing and their Applications (ISSPA), pp. 1319–1323, IEEE, Montreal, Canada, July 2012.
[9]. T.Mar,S.Zaunseder,J.P.Mart´ınez,M.Llamedo,andR.Poll, “Optimization of ECG classification by means of feature selection,” IEEE Transactions on Biomedical Engineering, vol. 58, no. 8, pp. 2168–2177, 2011.
[10]. J. Deepu et al., “A 3-lead ECG-on-chip with QRS detection and lossless compression for wireless sensors,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 12, pp. 1151-1155, Dec 2015.