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Implementation of Basic Reversible Logic Gates using Quantum Dot Cellular Automata

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Abstract: Quantum-dot Cellular Automata (QCA) is attaining worldwide recognition of researchers for its outstanding efficiency in terms of size, energy consumption, and latency as compared to similar nanotechnologies like Complementary Metal-Oxide-Semiconductor (CMOS), a Single Electron Technology (SET), nanowire transistor, Carbon Nanotube Field-Effect Transistor (CNTFET) [1]. The productive implementation of reversible logic is very crucial to carry out quantum computing. Reversible logic reduces the number of gates, quantum cost, and garbage output as information lost during the computation is zero. Reversible logic is an invertible process which means that for each final state of the system, a unique initial state can be determined. There are various implementations of Reversible Logic Gates and Quantum Computing in today's world, viz., DNA computing, low power CMOS, nanotechnology, etc. This paper provides efficient and modified designs of seven reversible gates using Quantum-dot Cellular Automata.

Keywords: Reversible Logic Gate, Quantum-dot Cellular Automata, Quantum Computing, VLSI.

I. INTRODUCTION

Energy dissipation in logic circuits became one of the major issues with the advancement in technology. R Landauer [2] in 1960 demonstrated that this dissipation is due to the loss of information in complex circuits that use irreversible gates. According to his principle, k*T*ln2 joules of energy per bit of information is dissipated in irreversible logic gates where Boltzmann's constant is denoted by 'k' and the absolute temperature is denoted by 'T'. To overcome this problem C.H. Bennett [3] recommended the use of reversible logic gates as they have equal numbers of inputs and outputs. According to Moore's law [4], the numbers of transistors will double every 18 months. Thus, the need for energy conservative devices is important. The amount of energy dissipated is correlated to the number of bits erased during computation. To overcome this complication and continue the trend of miniaturization of gadgets, QCA technology is used as an alternative as it is a transistor less approach. QCA uses a pattern of coupled quantum dots to realize different logic functions. For physical implementation, it uses quantum mechanical phenomena. A reversible logic gate is a memory-less logic fundamental that realizes an injective logical function that allows the input and output to have a one-to-one mapping [5], therefore no information is lost while transmission.

II. LITERATURE SURVEY

Bennett in the year 1973 showed how the use of a reversible gate for designing a logical circuit would considerably reduce the heat loss of KT ln 2 which was there in the case of irreversible gates. This eliminated the issue related to heat but the alarming increase of transistors in a circuit as stated by Gordon Moore in 1975 still needed to be considered. To eradicate this, QCA technology was taken into consideration as uses cells as an alternative to traditional transistors. Reversible gates in QCA technology is by far the best way to implement a logic circuit and designing digital circuits. Many reversible gates have been proposed in the last two decades by several researchers. In this paper, we have proposed some reversible gates which are more efficient than what was proposed earlier. The gates proposed in this paper are R gate [6] which is used to invert and duplicate a signal, BJN gate [7] which is a modified Tofolli gate [8] used as a universal gate, URG [9], and MCL [10] gates which are 3*3 gate. Some 4*4 gates are also proposed, they are PTR gate [11] which can be used as a reversible full adder, HNG gate [12] that can be used to design ripple carry adder, and MTSG[13] gate which can be used as an alternative to TSG gate [14] is it has a lower quantum cost.

III. REVERSIBLE LOGIC

Reversible logic is a promising technique for designing circuits with no heat dissipation. It depends upon entropy, heat transfer, the probability of a quantum particle, and the electrodynamics between electrons in a system [15]. Reversible logic has the same number of inputs and outputs which gives one-to-one mapping and it allows no fan out. They have the least value of quantum cost and garbage output. They are the basic building block of quantum computers. It can be best implemented in the QCA technique which uses an electron-dot to implement a circuit. QCA is based on a cell

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structure where each cell serves as a bit, it consists of four quantum dots and two electrons charge. The two charges can only be placed in two quantum sites diametrically to each other due to the Colombian effect between the charges. This creates an internal effect which gives rise to two possible configurations which represent two binary states '0' and '1'. This force of repulsion is solely responsible for the transmission of values.

IV. REVERSIBLE LOGIC AND THEIR QCA IMPLEMENTATION

In the sections below we have discussed some reversible gates and their simulations using QCA Designer [16], a tool used for simulation.

a. R GATE

It is a 3*3 gate that has A, B, and C as input and P, Q, and R as output where P=A ⊕ B, Q=A, and R=C' ⊕AB. Figure A below shows the circuit diagram and simulation in QCA.

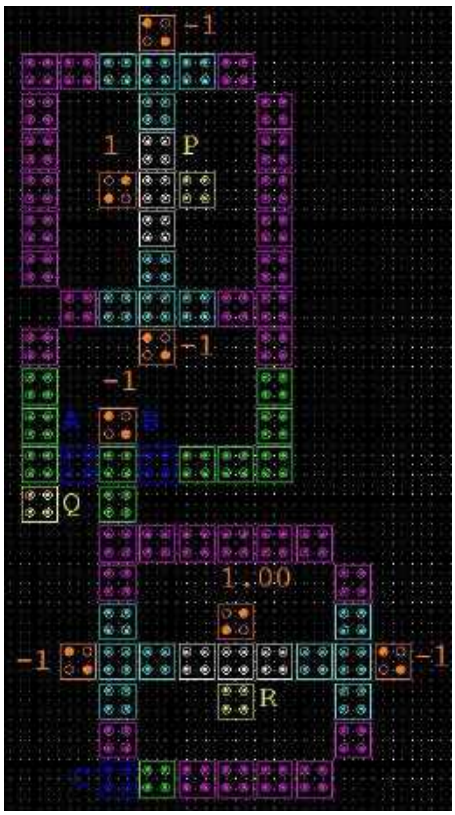

Fig (1) QCA implementation of R gate

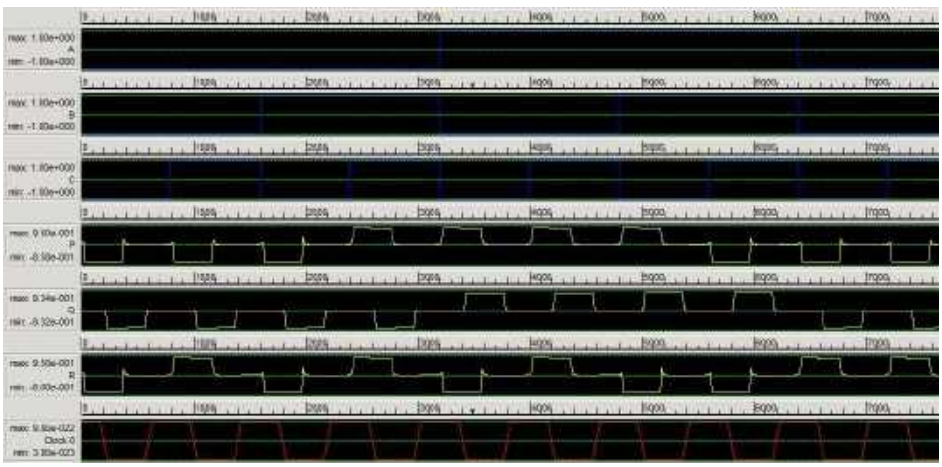

Fig 2: Simulation output waveform of R gate

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b. URG GATE

It is a 3*3 gate that has A, B, and C as input and P, Q, and R as output where P= (A+B) ⊕ C, Q=B, and R=AB ⊕C. Figure B below shows the circuit diagram and simulation in QCA.

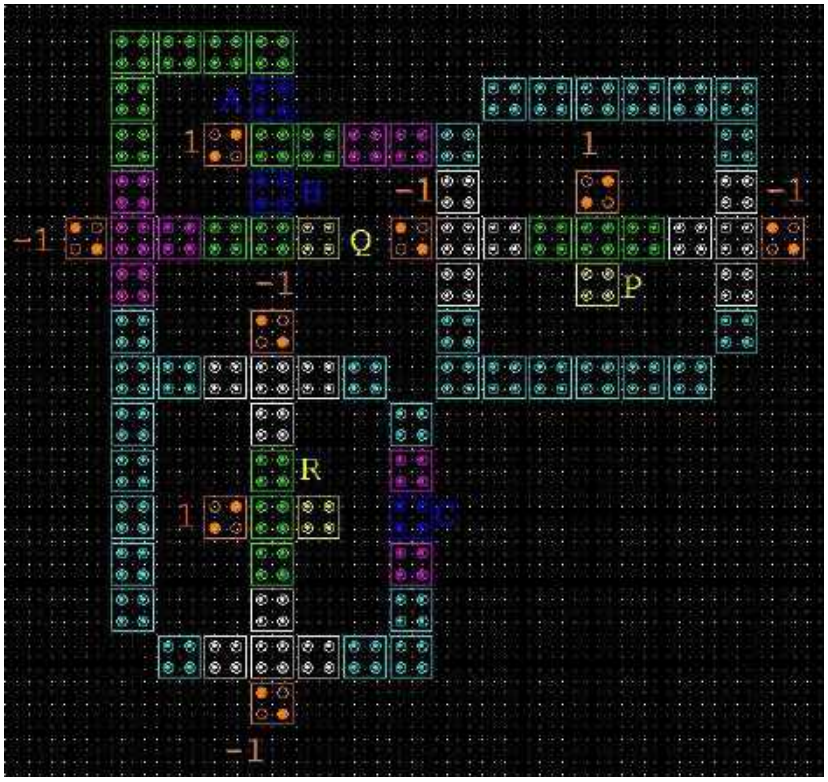

Fig 3: QCA implementation of URG gate

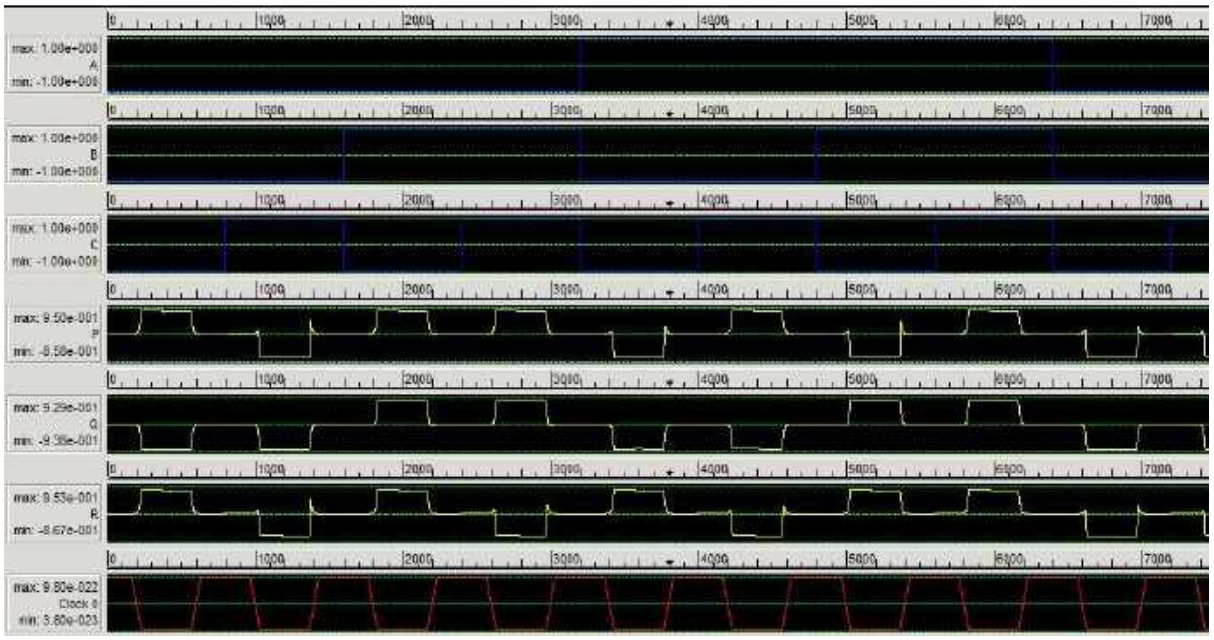

Fig 4: Simulation output waveform of URG gate

c. MCL GATE

It is a 3*3 gate that has A, B, and C as input and P, Q, and R as output where P= (B+C)', Q= (A+B)', and R=A. Figure A below shows the circuit diagram and simulation in QCA.

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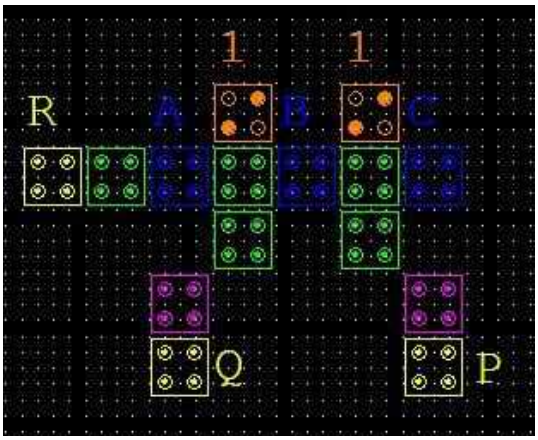

Fig 5: QCA implementation of MCL gate

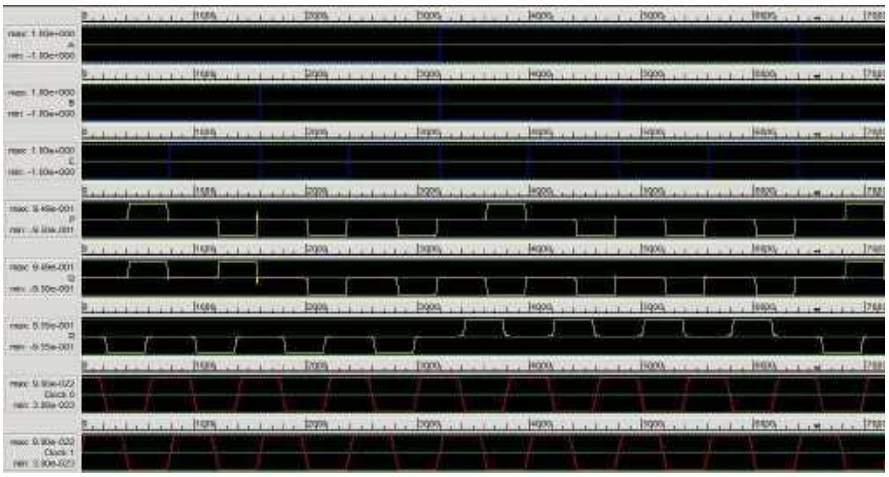

Fig 6: Simulation output waveform of MCL gate

d. PTR GATE

It is a 4*4 gate that has 0, A, B, and C as input and P, Q, and R as output where P= (A ⊕ B)', Q=A⊕B⊕C, and R= C (A⊕B)+AB and S=A'(B⊕C)+BC. Figure D below shows the circuit diagram and simulation in QCA.

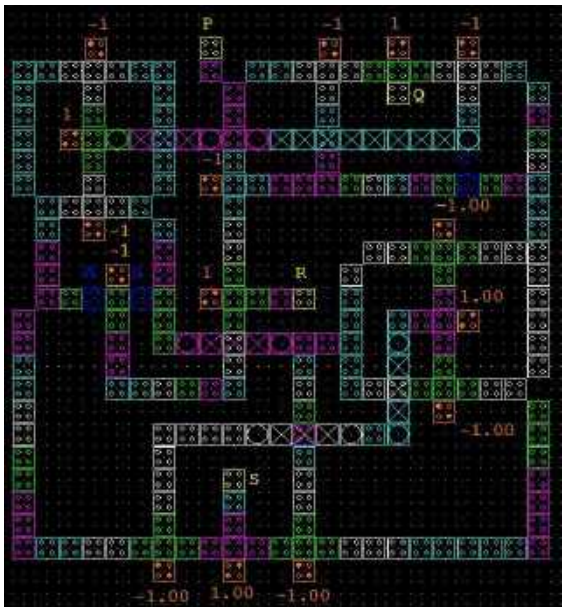

Fig 7: QCA implementation of PTR gate

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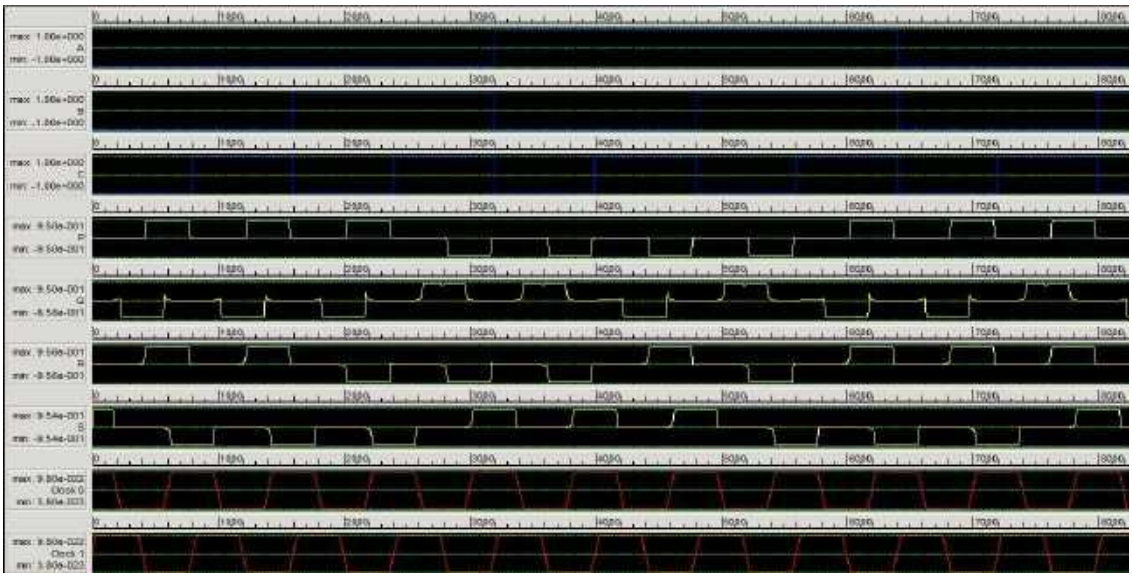

Fig 8: Simulation output waveform of PTR gate

e. HNG GATE

It is a 4*4 gate that has A, B, C, and D as input and P, Q, and R as output where P=A, Q=B, and R=A⊕B⊕C and S= (A⊕B).C⊕AB⊕D. Figure E below shows the circuit diagram and simulation in QCA.

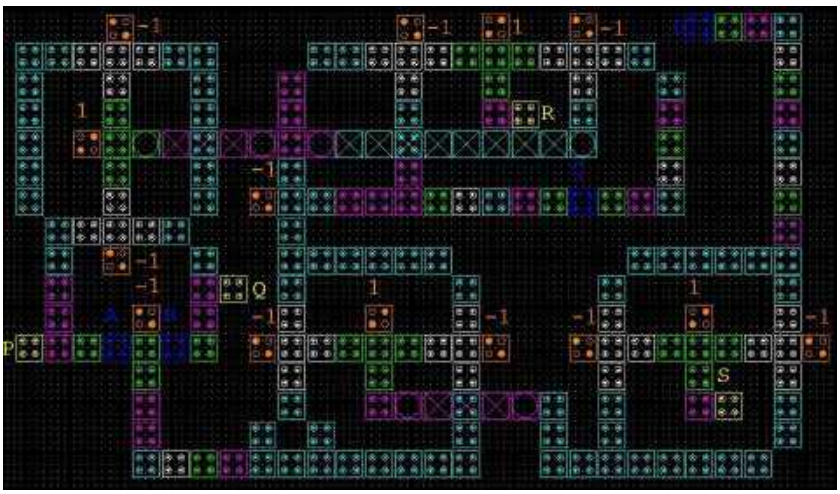

Fig 9: QCA implementation of HNG gate

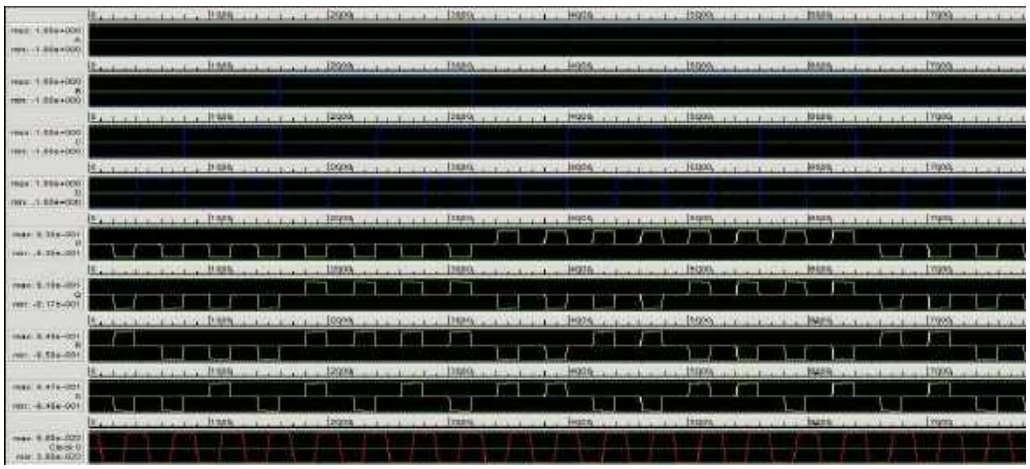

Fig 10: Simulation output waveform of HNG gate

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f. MTSG GATE

It is a 4*4 gate that has A, B, C, and D as input and P, Q, R and S as output where P=A, Q=A⊕B, and R=A⊕B⊕C and S=(A⊕B)C+AB⊕D. Figure F below shows the circuit diagram and simulation in QCA.

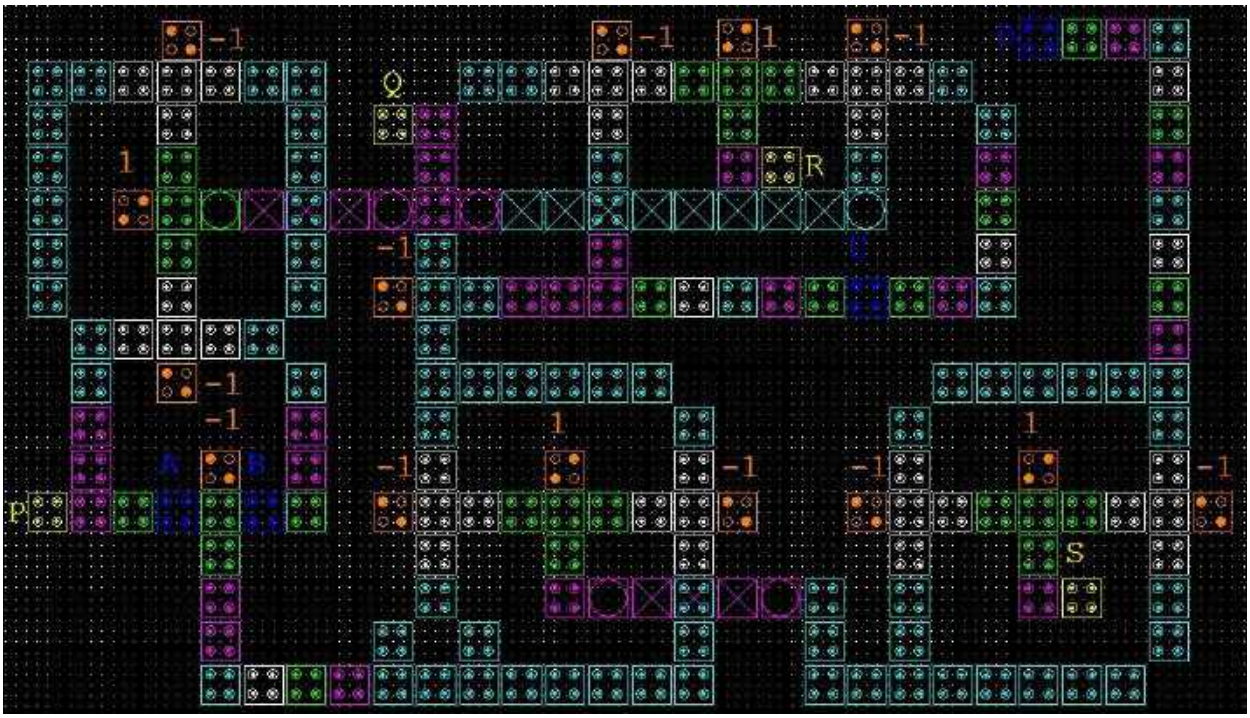

Fig 11: QCA implementation of MTSG gate

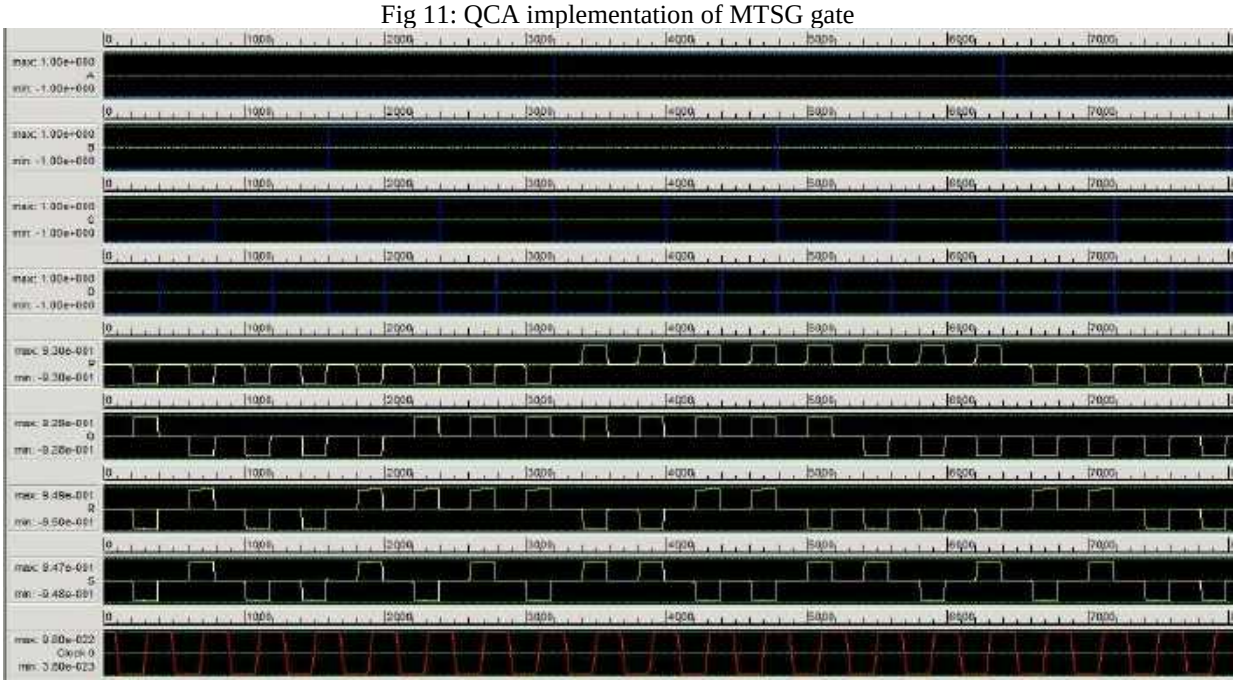

Fig 12: Simulation output waveform of MTSG gate

g. BJN GATE

It is a 3*3 gate that has A, B, and C as input and P, Q, and R as output where P=A, Q=B, and R= (A+B) ⊕C. Figure G below shows the circuit diagram and simulation in QCA.

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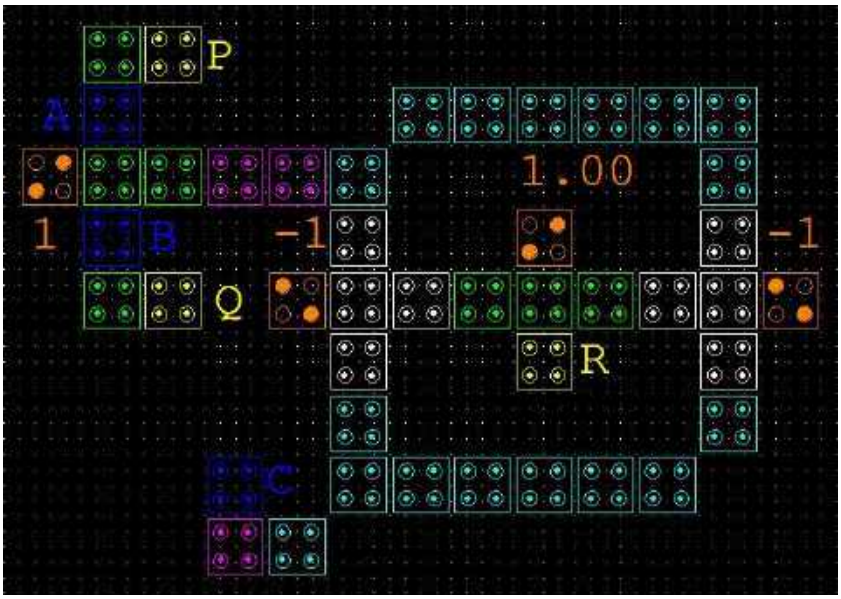

Fig 13: QCA implementation of BJN gate

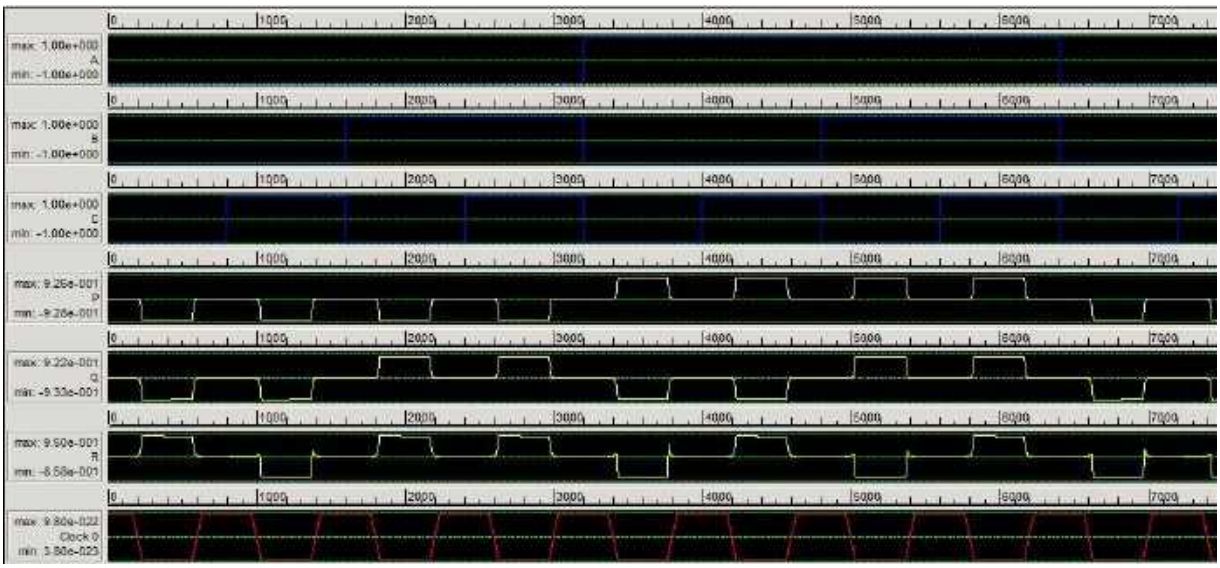

Fig 14: Simulation output waveform of BJN gate

V. COMPARITIVE STUDY

A comparative analysis of gates in terms of complexity which defines the number of cells used, the area covered, delay during propagation, and the time taken while designing and simulation of the proposed design and previous design is shown in the tables below. In table VIII, the parameters of different gates proposed by us is shown. The proposed R, URG, MCL, PTR, HNG, MTSG, and BJN gates are more efficient than the papers published earlier in terms of space requirement and time taken by them during the simulation.

TABLE I: Comparison of parameters of R Gate

	Previous work [17]	Proposed work
Complexity (No. of cells used)	105	78
Area (in µm2)	12.3	0.091614
Delay (clocking zones)	0.75	3
Simulation time (in seconds)	-	2

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TABLE II: Comparison of parameters of URG Gate

	Previous work [18]	Proposed work
Complexity (No. of cells used)	114	84
Area (in µm2)	0.078	0.111810
Delay (clocking zones)	1	4
Simulation time (in seconds)	-	2

TABLE III: Comparison of parameters of MCL Gate

	Previous work [19]	Proposed work
Complexity (No. of cells used)	16	15
Area (in µm2)	0.017	0.018765
Delay (clocking zones)	1	2
Simulation time (in seconds)	-	2

TABLE IV: Comparison of parameters of HNG Gate

	Previous work [20]	Proposed work
Complexity (No. of cells used)	420	219
Area (in µm2)	-	0.18367
Delay (clocking zones)	-	13
Simulation time (in seconds)	-	3

TABLE V: Comparison of parameters of MTSG Gate

	Previous work [20]	Proposed work
Complexity (No. of cells used)	420	219
Area (in µm2)	-	0.18367
Delay (clocking zones)	-	-
Simulation time (in seconds)	-	3

TABLE VI: Comparison of parameters of BJN Gate

	Previous work [21]	Proposed work
Complexity (No. of cells used)	48	45
Area (in µm2)	0.0525	0.052332
Delay (clocking zones)	0.75	4
Simulation time (in seconds)	-	2

TABLE VII: Comparison of parameters of different proposed gates

Gate	Complexity (No. of cells used)	Area (in $\mu m^{2)}$	Delay (clocking zones)	Simulation time (in seconds)
R	78	0.091614	3	2
URG	84	0.111810	4	2
MCL	15	0.018765	2	2
PTR	265	0.24141	10	3
HNG	219	0.18367	13	3
MTSG	219	0.18367	-	3
BJN	45	0.052332	4	2

VI. CONCLUSION

The reversible logic gates proposed in this paper are done considering the optimum number of Q cells required for the design. We have also considered space complexity. Thus, the proposed designs have also consumed the optimum space required for the design. We assume that the proposed designs of reversible logic gates will consume considerably less

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amount of energy during operation and efficiency of compactness or integration could be increased compared to that of the designs proposed in previous research papers. In this paper, we have designed seven reversible logic gates, namely, BJN gate, HNG gate, MCL gate, MTSG gate, PTR gate, R gate, and URG gate. Many of these gates can be used as full adders. PTR gate can singly act as a CLA adder. However, gates like HNG and MTSG can be used as a CLA adder after connecting with few other gates like MCL, URG, etc. This paper may be used to design basic adder circuits using QCA at optimum requirements with maximum efficiency.

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