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ASYMMETRICAL MULTILEVEL INVERTER WITH ADVANCED PWM TECHNIQUES

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Abstract – In this paper a "Asymmetric Multilevel inverter with advanced PWM techniques" is proposed Proposed MLI includes single source, less range of switches, diodes, and capacitors, total harmonic distribution, harmonic spectrum. As such per simulation result as we increase the voltage level of inverter, the harmonic will reduced. Implementation of Asymmetrical Multilevel with advanced PWM techniques by using MATLAB/SIMULINK.

Key words: MLI Simulation, PDPWM, PODWM, APODPWM method, THD.

I .INTRODUCTION

Multilevel Converters are finding increased attention in industry and academia as one of the preferred choices of electronic power conversion for high power applications. They have successfully made their way into the industry and therefore considered as a mature and proven technology. The concept of multilevel converters has been introduced since 1975. The cascaded multilevel inverter was first proposed in 1975. The term multilevel begin with three-level converter. In 1981, diode clamped multilevel inverter also called neutral point clamped (NPC) inverter schemes were proposed. In 1982, capacitor clamped (flying capacitor) and in 1996

II. PROPOSED TOPOLOGY

This dissertation presents a new topology based on asymmetrical multilevel inverter. This proposed topology has reduced number of switches and lower harmonic distortion in the output voltage in comparison to conventional multilevel inverter topology. It consists of two voltage source (V_1 and V_2) with different magnitude and six unidirectional switches (S1, S2, S3, S4, S5, S6.)

1. Operation of a Proposed 7 Level Asymmetrical MLI Topology

producing 7 levels in output voltage, proposed topology required two voltage source (V_1 and V_2) with different magnitude and six
unidirectional switches (S_1, S_2, S_3, S_4, S_5, and S_6). For generating all positive and negative levels, magnitude of voltage sources (V_1 : V_2) should be in the ratio (1 : 2). it is clear that the switching combinations (S_1, S_2), (S_3, S_4), and (S_5, S_6) should not be turned 'ON' simultaneously.

Fig. 1 General structure of proposed topology 7-level

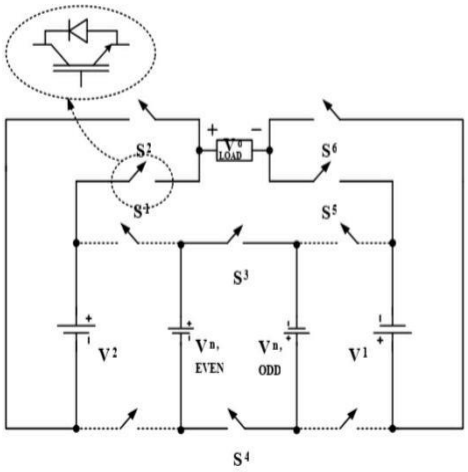

TABLE 1. Switching Scheme of Proposed Asymmetrical MLI

State	Switching Scheme						Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	
1	ON	OFF	OFF	ON	ON	OFF	V_2+V_1
2	ON	OFF	OFF	ON	OFF	ON	V_2
3	OFF	ON	OFF	ON	ON	OFF	V_1
4	OFF	ON	OFF	ON	OFF	ON	0
5	ON	OFF	ON	OFF	OFF	ON	$-V_1$
6	OFF	ON	ON	OFF	ON	OFF	$-V_2$
7	OFF	ON	ON	OFF	OFF	ON	$-(V_2+V_1)$

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2. Operating Modes of Proposed 7-level Asymmetrical MLI

Fig. 2 (a-g) are the different operating modes of ASMLI

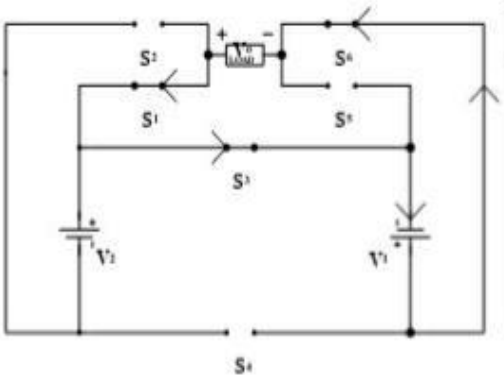

Fig .(a) (V2+V1)

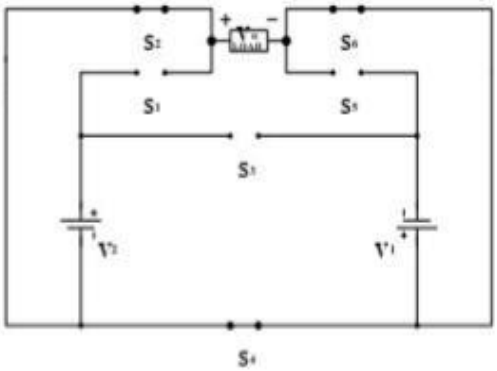

Fig. (b) (V2)

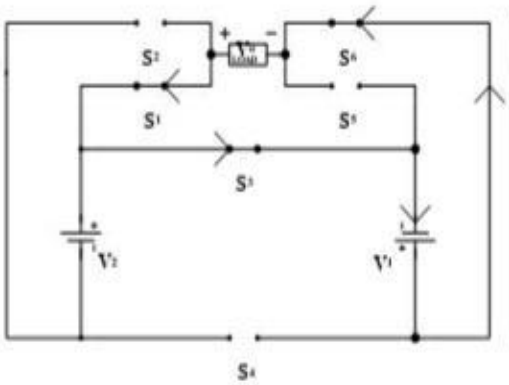

Fig.(c) (V1)

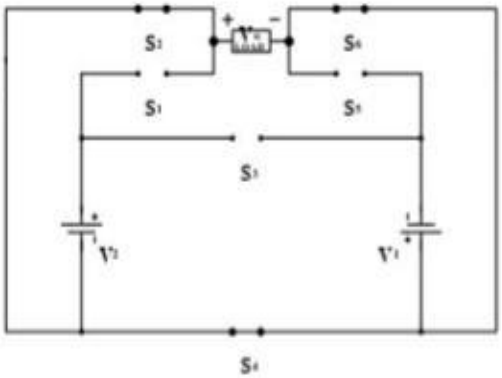

Fig. (d) (0)

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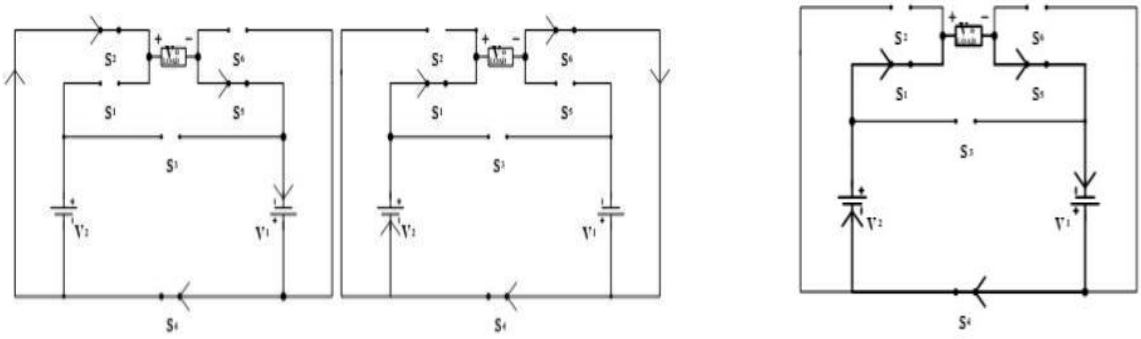

Fig.(e) -(V1) Fig. (f) (-V2) Fig. (g) –(V2+V1)

III. .SIMULATION OF PROPOSED 7-LEVEL ASMLI TOPOLOGY

Proposed 7-Level MLI is simulated with the help of MATLAB/Simulink R2013a software version. The simulation parameters for 7-Level MLI are as follows: Resistance R=10 Ω, and DC Voltage sources are V_1=50V & V_2=100V.Frequency of carrier signal is 2 kHz and Frequency of Reference signal is 50 Hz. For harmonics calculations, Frequency Modulation (M_f) is 40, and Modulation Index (M_a) is variable.

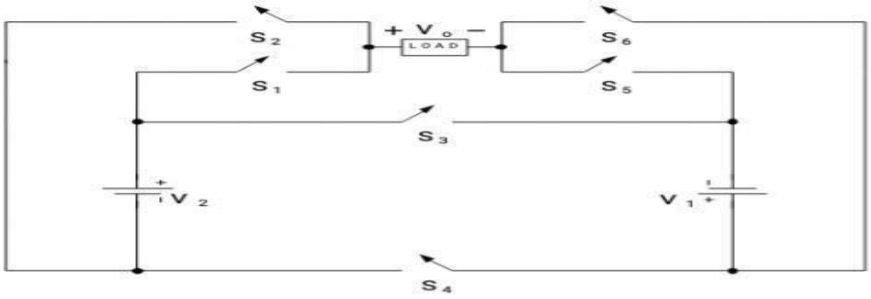

Fig. 3 Model of single- Phase 7-Level Asymmetrical MLI

IV. SIMULATION RESULTS

Fig.4 shows the output phase voltage result of a 7-level MLI with PODPWM technique. Table2 represents THD at different modulation index. For 7- level MLI, corresponding THD in % are shown in Fig.

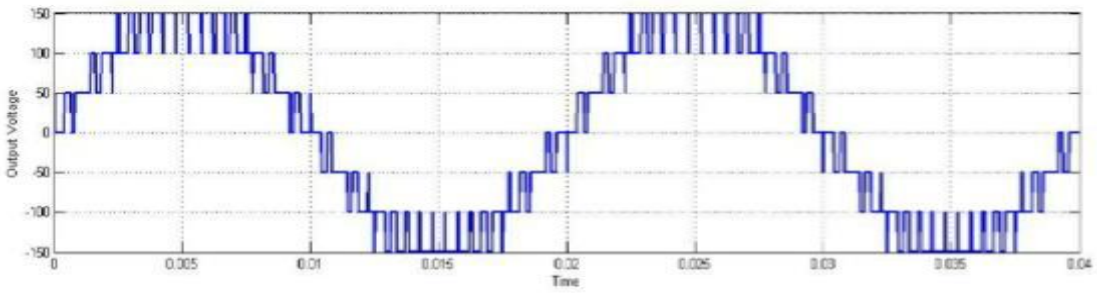

Fig.4. Output Voltage Waveform of Proposed 7-Level Asymmetrical MLI

Comparative analysis of THD for different PWM techniques . For 7-level MLI, corresponding Total Harmonic distortion in % (% THD) PD= 18.23, POD= 18.18, APOD=18.39 at modulation index (Ma) = 1.0

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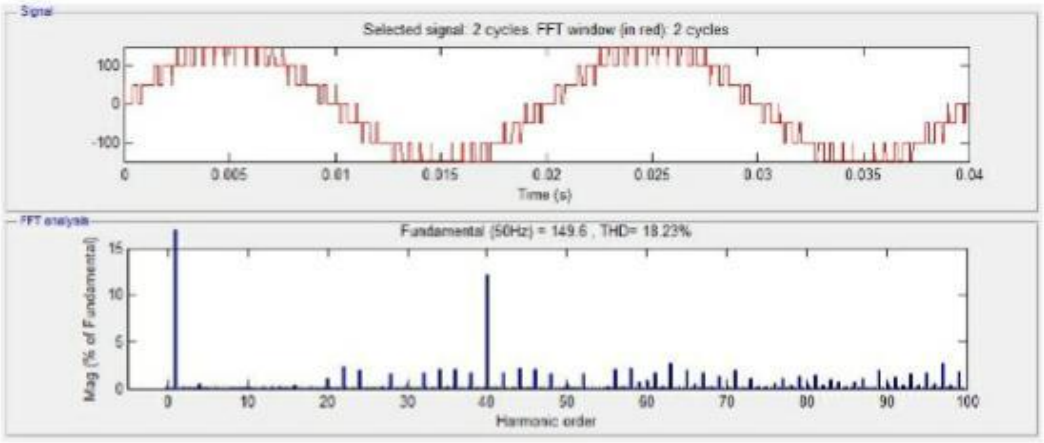

Fig 5.THD of 7-Level ASMLI PDPWM for R-Load (Ma=1.0&Mf=40)

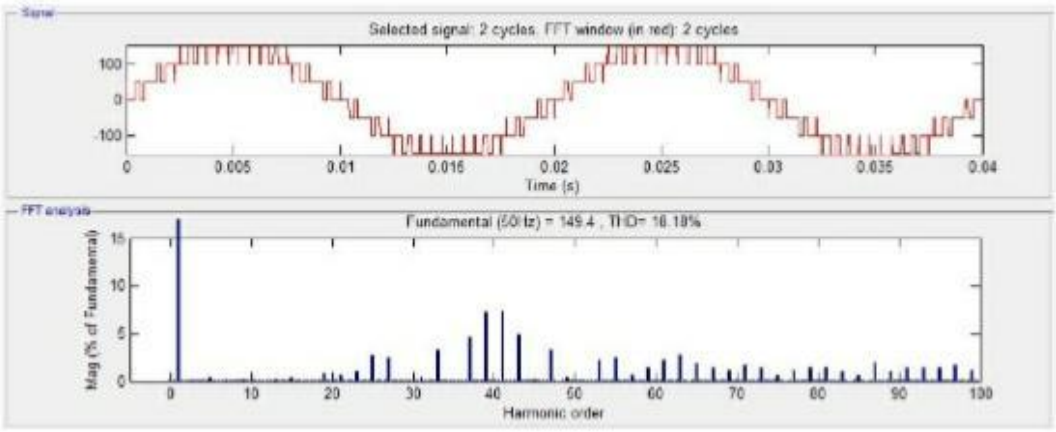

Fig. 6. THD of 7-Leve ASMLI PODPWM for R-Load (Ma =1.0&Mf=40)

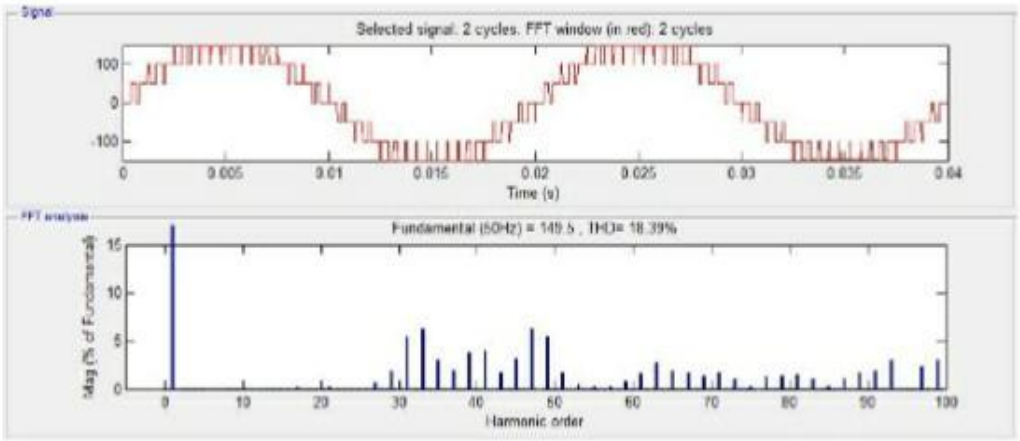

Fig.7.THD of 7-Leve ASMLI APODPWM for R-load (Ma=1.0&Mf=40)

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TABLE- 2. Comparative THD analysis of different PWM techniques for 7-level ASML6.

V. CONCLUSION

Modulation Index	PDPWM	PODPWM	APODPWM
1	18.23	18.18	18.39
0.95	20.59	20.60	20.23
0.90	22.40	22.11	21.98
0.85	23.62	23.49	23.25
0.80	24.30	24.07	24.19

The Asymmetrical proposed topology for 7-level MLI are implemented. For 7-level the % THD result is shown in Table 2 respectively with different PWM techniques and modulation indices. From these results it can be concluded that with the increase of number of level of output near sine wave is obtained which offers less THD and less distortion. The simulation results for 7- level with asymmetrical MLI topology are presented in this . The value of harmonic distortion have been calculated at different modulation index and PWM techniques.

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