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Reverse Voltage Topology For Multilevel Inverters

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Abstract: In this paper a "Reverse Voltage Topology for Multilevel Inverter" is proposed. The advancements in semiconductor technology, multilevel inverter technology is widely employed for megawatt power and medium voltage energy control applications. Construction of multilevel inverter is similar to single and three phase inverters. These inverters do not use a transformer for their operation, reduce harmonic losses and give less disturbance Since. The simulation results are provided for 5-level R-V Topology with In-Phase Disposition (IPD) and Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD). Finally, output voltage and currents are demonstrated by simulation.

Keywords: Reverse Voltage Topology, Multilevel Inverter, THD, PWM Techniques.

I. INTRODUCTION

The concept of multilevel inverter was introduced since from1970s. The term multilevel inverter basically starts with three voltage levels that can used in high power medium voltage application due to its advantage over the two level inverter. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor, switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Different multiple DC voltage sources like Capacitors, batteries, and renewable energy voltage sources can be used in multilevel inverter.

The word “Multi-level inverter” has become more popular, due to its rising demand in the industry because they provide reduced energy consumption, improved product quality, better system efficiency, good maintenance, and many more. Conventional two-level inverters, are used to generate an AC voltage from DC voltage supply. The two-level inverter can only create two different output voltages for the load, Vdc/2 or -Vdc/2. To build up an AC output voltage these two voltages are usually switched with PWM. But two-level inverter is effective it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage three different multilevel converter structures have been useful in industrial applications. Cascaded H-bridges converter with separate dc sources, Diode clamped, Flying capacitors each type of multilevel converters distribute the advantages of multilevel voltage source inverters, they may be opposite for detailed application due to their structures and drawbacks. In a multilevel VSI, the dc-link voltage Vdc is obtained from any tools which can acquiesce stable dc source. Series connected capacitors provided that some nodes to which multilevel inverter can be related. Mostly, the series connected capacitors will be assumed to be any voltage sources of similar value. Each capacitor voltage Vc is specified by Vc = Vdc/(n-1), where n is number of level.

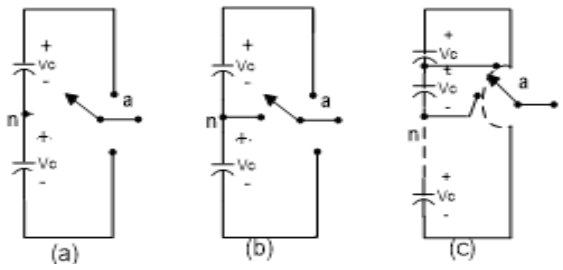

Fig. 1: one phase leg of inverter (a) two level (b) three level (c) n-levels

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II. MODULATION TECHNIQUES

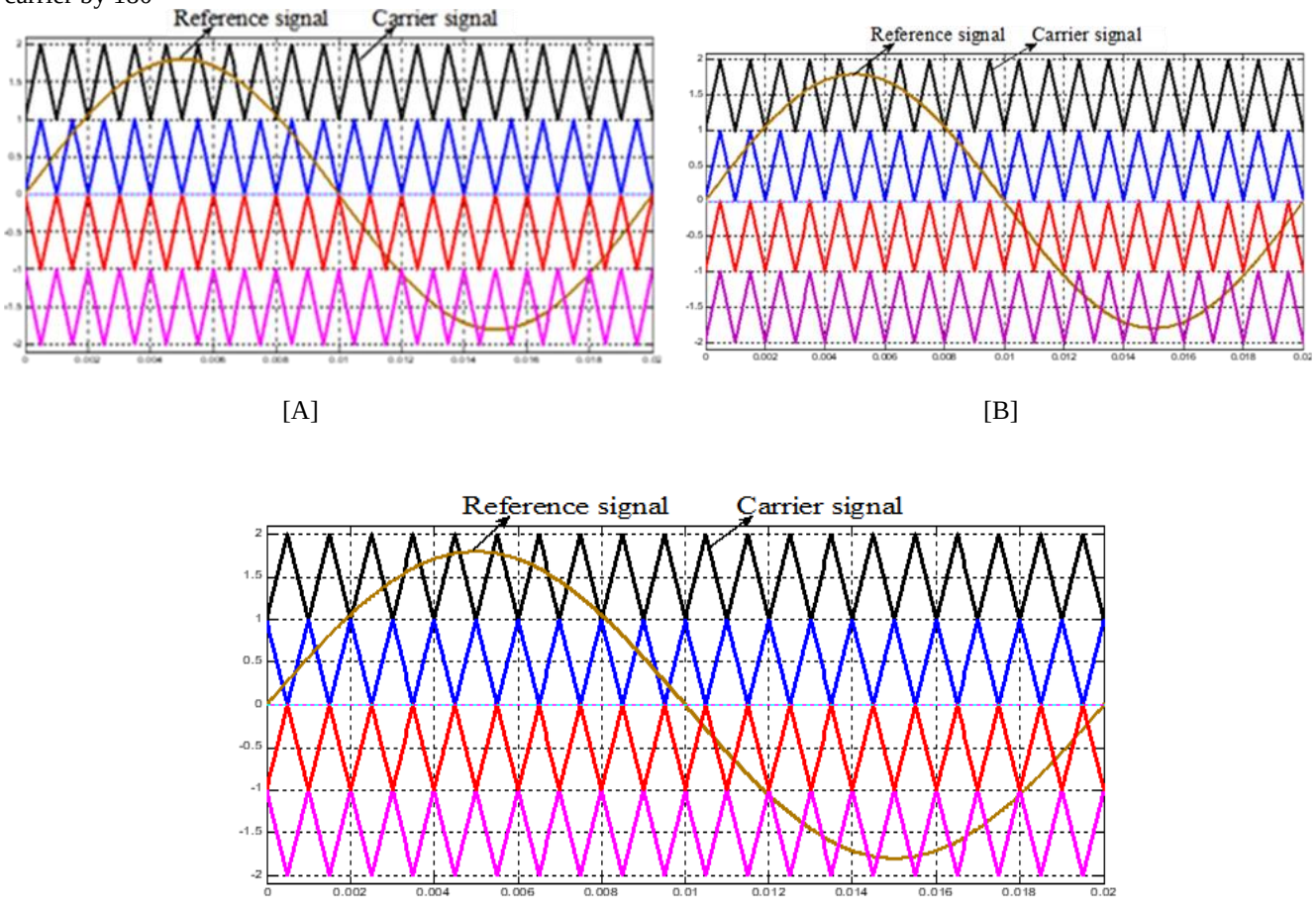
The power electronic converters are operated in the "switched mode". Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal.

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. An n-level proposed inverter using level-shifted and phase-shifted multicarrier modulation scheme requires (n-1) triangular carriers, all having the same frequency and amplitude. There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation.

[A] In-phase disposition (IPD), where all carrier waveforms are in phase

[B] Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.

[C] Alternate phase opposition disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 180^0



[A] [B]

[C]

Fig. 2: Carriers and modulating signals at mf = 20, ma = 0.9.
For [A]: Phase Disposition
For [B]: Phase Opposition Disposition
For [C]: Alternate Phase Opposition Disposition

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III.PROPOSED METHODOLOGY

This paper presents an overview of a proposed multilevel inverter topology with H-bridge and auxiliary switches. This topology requires less number of components & less gate driver circuits as compared to conventional multilevel inverter topologies and avoids voltage balancing problems. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. This topology is also required lower (%) THD in comparison of other MLI topologies.

The block diagram of 5-level multi-level inverter using this topology is shown in Fig.4. The principal idea of these topology as a multilevel inverter is that the left stage in generates the required output levels (without polarity) and the right circuit H-bridge (full-bridge converter) decides about the polarity of the output voltage. This H-bridge part transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity

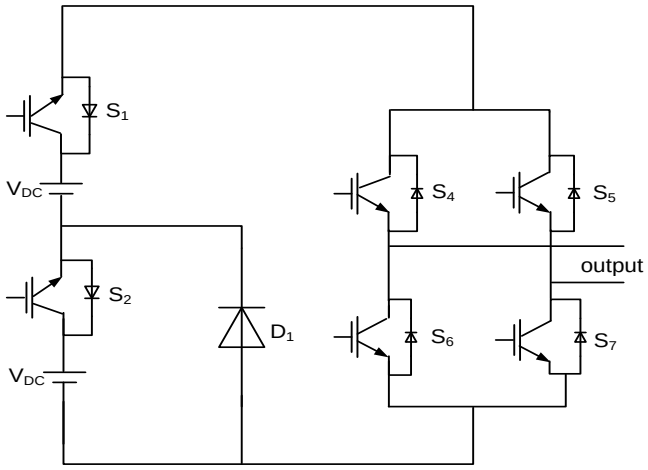

Fig.3: Single Phase 5-level RV MLI

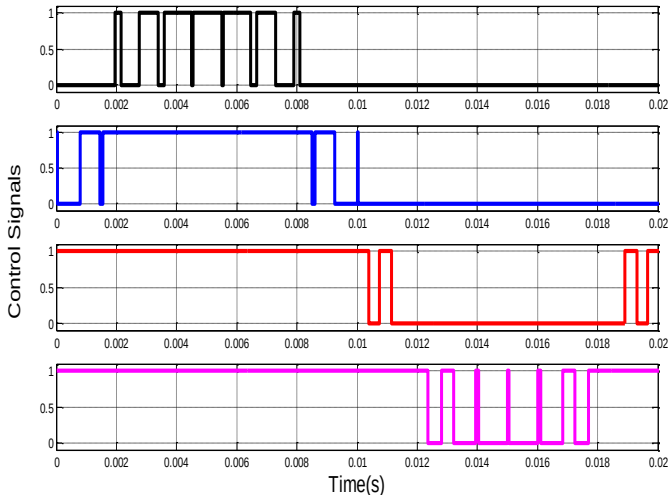

Fig.4: [A] Carriers and Modulating Signal at mf=20, ma=0.9 for Phase Disposition

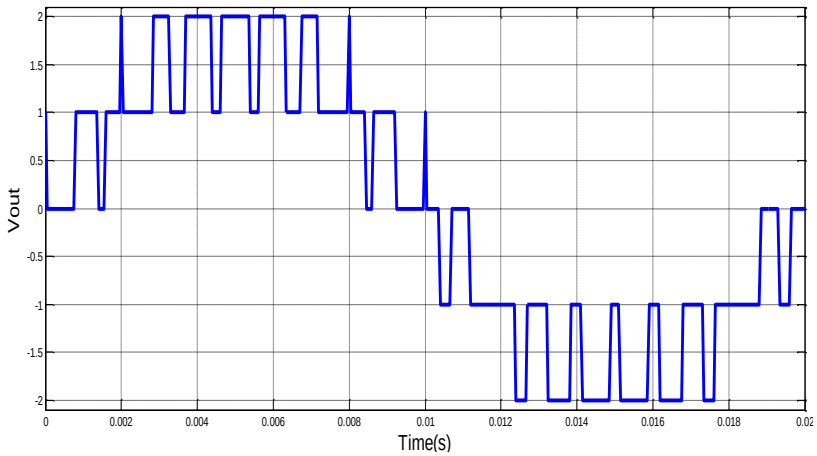

Fig.4: [B] Output Phase Voltage (Vout) For Phase Disposition

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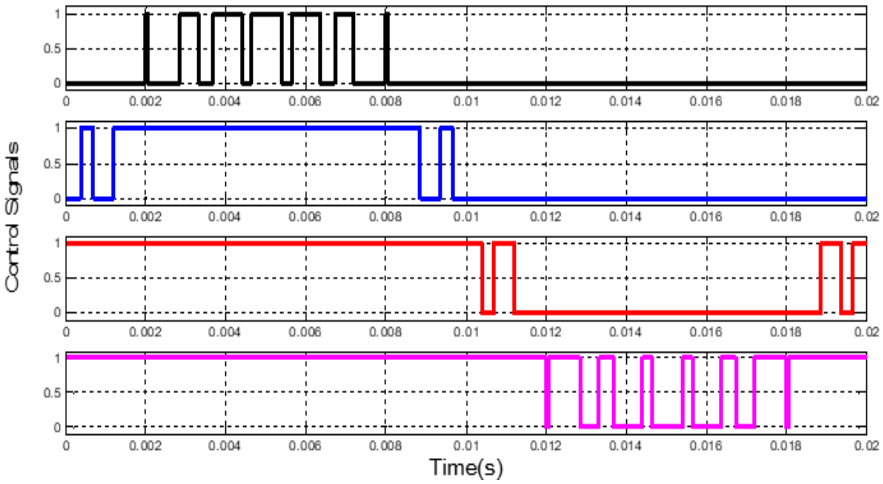

Fig. 5: (A) Carriers and modulating signals at mf = 20, ma = 0.9
For Phase Opposition Disposition

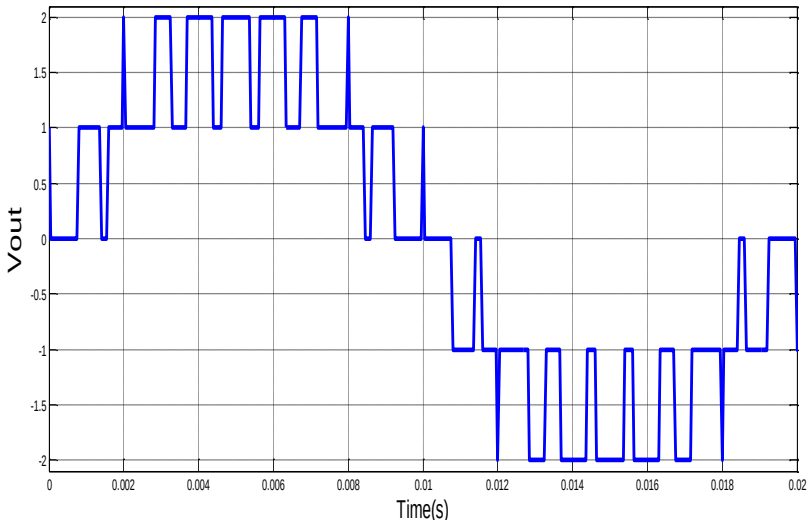

Fig. 5: (B) Output Phase Voltage (Vout)
For Phase Opposition Disposition

IV. SIMULATION MODEL AND RESULTS WAVEFORM

Five level MLI is simulated with the help ofMATLAB/Simulink. Here the sub system for pulse generator is modelled where one reference wave (sine wave) and four carrier waves (triangular wave) are taken. Two of them are applied across the positive half cycle of the modulating signal, remaining two of them are applied across the negative half cycle of the modulating signal (sine wave).

Based on the concepts explained in modulation techniques, eight pulses are generated. Theses pulses are given to the switches in one phase leg of a five level inverter.

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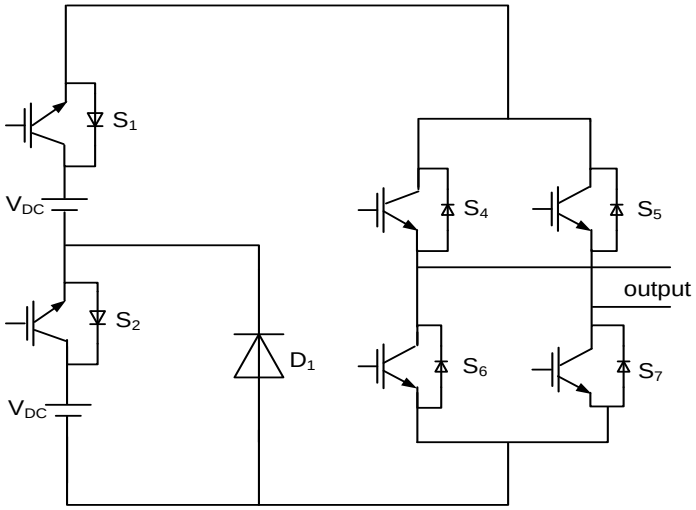

Fig.6: Model of single-Phase Five-level RV MLI

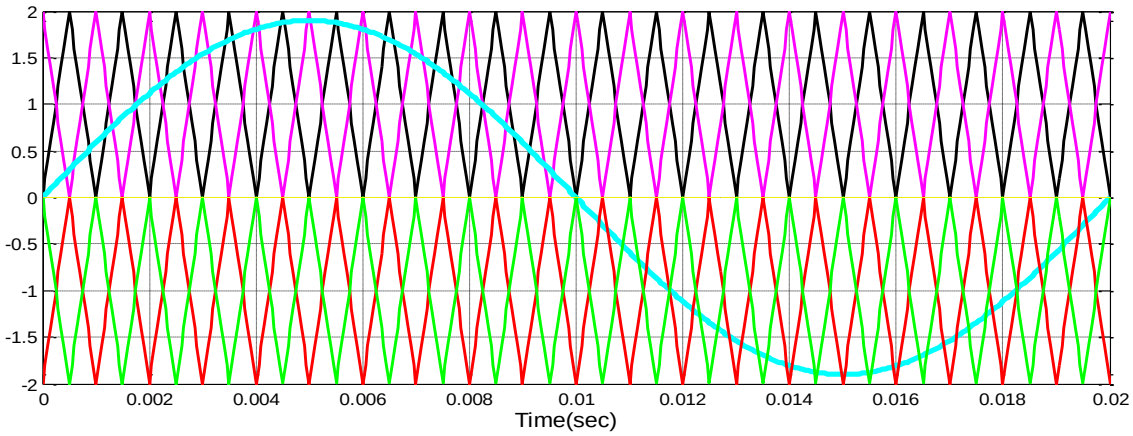

Fig.7: [A] Carrier Modulation Signals of single-Phase 5-Level MLI

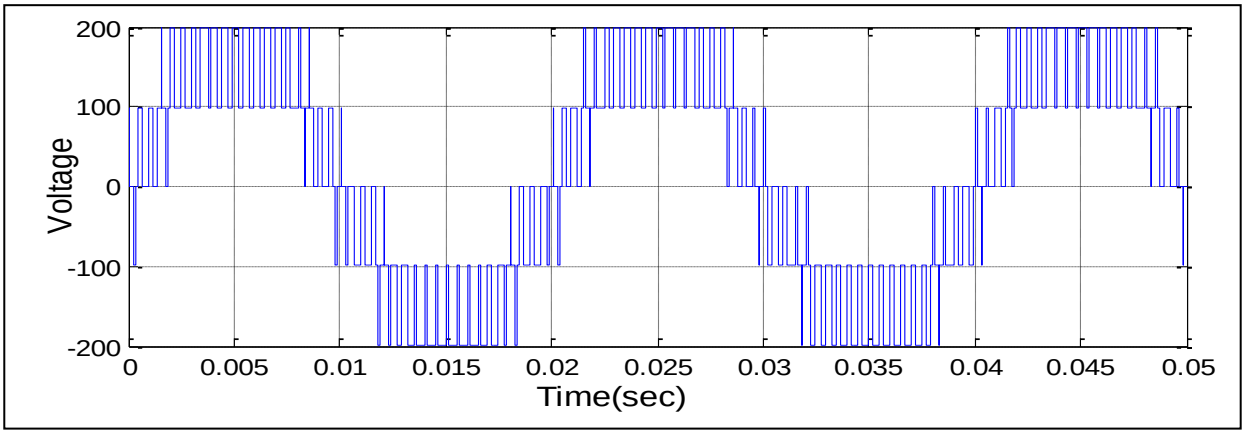

Fig.7: [B] Output Phase Voltage of a 5-level MLI for R-L Load.

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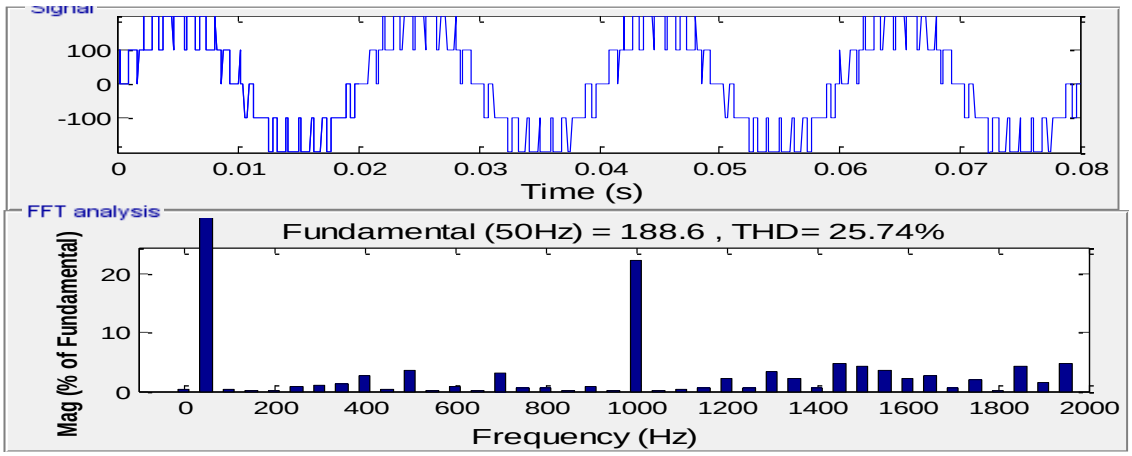

Fig.8: Phase output voltage by PDPWM for R-L load (Ma=0.9, Mf=20)

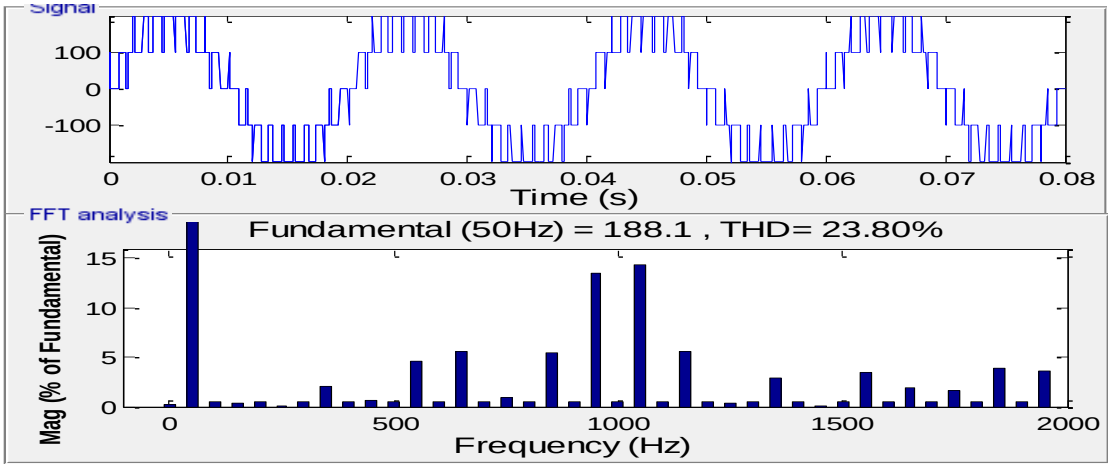

Fig.9: Phase output voltage by PODPWM for R-L load (Ma=0.9, Mf=20)

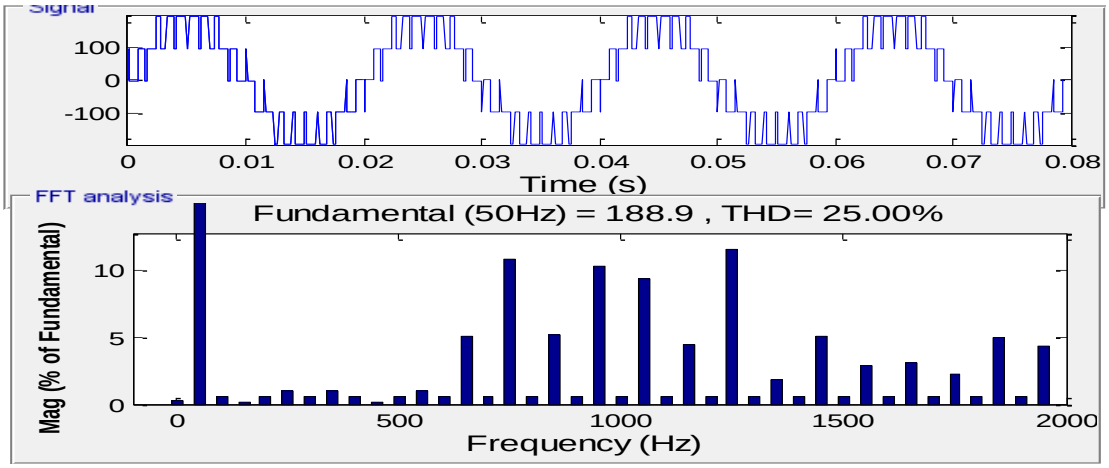

Fig.10: Phase output voltage by APODPWM for R-L load (Ma=0.9, Mf=20)

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TABLE I: Comparative THD analysis of different PWM techniques for 5-level MLI

Modulation Index	POD PWM %THD	PD PWM %THD	APOD PWM %THD
1	22.38	20.42	21.20
0.9	25.74	23.80	25.00
0.8	29.26	28.17	28.98
0.7	32.09	31.78	31.52

V. CONCLUSION

Multi-level inverters 5- level has been simulated using MATLAB/Simulink. The following conclusions can be made from the analysis:-

In this thesis, a proposed topology has been used which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. In this thesis, a 5-level multi-level inverter using this topology is proposed with different PWM techniques and it is being found that the proposed MLI is the most promising alternative for industry application. The switching operation of this topology requires less number of switches, less gate drive circuits and higher reliability as compared to conventional MLI topologies. It is proved that, the proposed topology can effectively work as a multilevel inverter with a reduced number of switches for different PWM techniques. The different SPWM control method is used to drive the inverter.

The simulation results for 5-level with RV topology are presented in this thesis. Their harmonic analysis carried out by using MATLAB R2013a software version. THD values of this MLI have been calculated at different modulation index. Simulation results show the performance of single-phase and three-phase 5-level MLI with different PWM techniques.

FUTURE WORK

In this dissertation work proposed a 9-level proposed MLI topology in single phase. With the help of proposed MLI topology we will increase the voltage levels with less number of power switches, capacitors and diodes and compare with the DCMLI, CHBMLI and FCMLI. In future it is being proposed that the same MLI topology will fed with the induction motor drives using direct torque control.

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