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Design and Implementation of T-type Multilevel Inverter using Different PWM Techniques for Reduced Count of Switching Devices

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Abstract: In this paper a "Design and Implementation of T-type Multilevel Inverter using Different PWM Techniques for Reduced Count of Switching Devices". Semiconductor devices extending their area of application because they provide less consumption, improciency, Improved quality, better maintenance, and many more, A multilevel inverter circuit having different option in high power and medium voltage situations. It provides cost Efficient solutions of multilevel inverter not only attains high power ratings, but also provides the use of low power Rating applications in renewable energy sources such as photovoltaic [3], wind, and fuel cells which can be easily Connected with multilevel inverter system for high power application.

Key Words: Multilevel T-type Inverter , PWM Techniques, GTO,IGBT,IGCT, MLI Simulation, 5-level Topology .

1.INTRODUCTION

The advancement in power electronic devices, This may not always be a problem but for some applications there may be a need for low distortion in the output voltage. A multilevel inverter is a very vital for power electronic device in the region of high-power, high-voltage applications due to its advantage over the conventional two-level inverter such as, low switching frequency, hence reduction in switching losses, lower harmonic, low common mode voltage. Multi-level power transfer and it is provided more than two voltage levels to at can generate a multiple-step voltage waveform with less distortion, less switching frequency and higher efficiency.

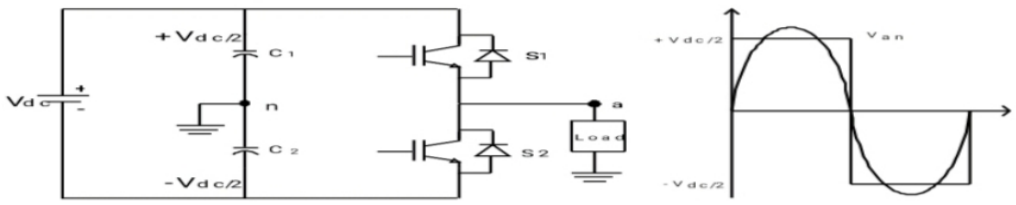

Figure 1.1 Circuit of Single Phase Two-Level Inverter and Two-Level Output Voltage Waveform

The quality of the output voltage is improved as the number of voltage levels increases, so the size of output filters can be decreased. The cascade multilevel inverter was first proposed in 1975.

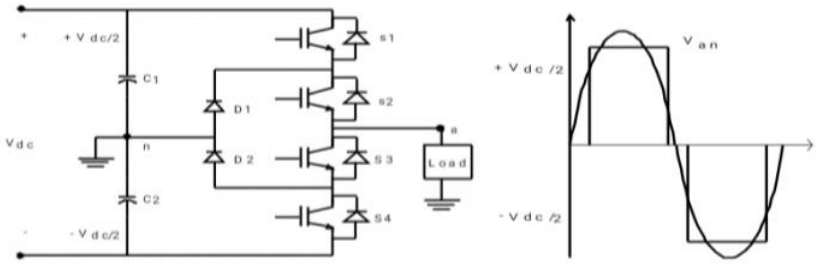

Figure 1.2 Circuit of Single Phase Three-Level Inverter and Three-Level Output Voltage Waveform

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2. CONVENTIONAL MULTILEVEL INVERTER SCHEMES

A three level converter is considered to be the least number in multilevel converter topologies. A multilevel converter can manage either its input or output nodes (or both)between multiple (more than two) levels of voltage or current. While the number of levels reaches infinity, the output THD approaches zero. Three different multilevel converter structures have been useful in industrial applications.

(a)Cascaded H-bridges converter with separate dc sources
(b)Diode clamped
(c)Flying capacitors

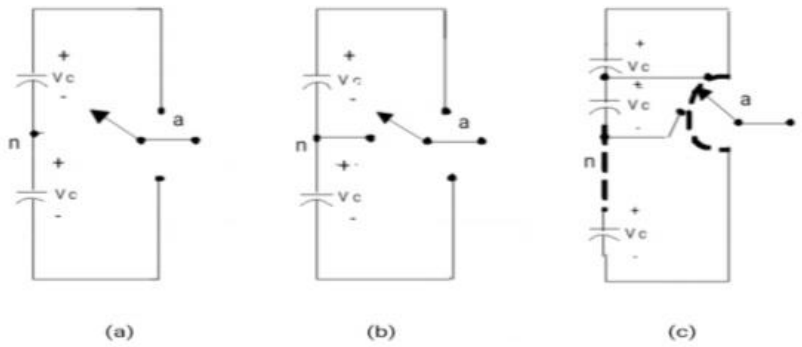

Figure 2.1 One Phase Leg Of Inverter (a) Two Level (b) Three Level (c) N-Levels

2.1.Diode-Clamped Multilevel Inverter: Diode-Clamped MLI Topology is a topology in which the diode is used as the clamping device to Clamp the dc bus voltage so the same as to achieve steps in the output voltage. The neutral point converter anticipated by Nabae, Takahashi, and Akagi, in 1981 was effectively a three-level diode- clamped inverter.

2.2. Cascaded H-Bridge Inverter: The Cascaded H-Bridge inverter is made up of multiple series string of single-phase full bridge inverters. Fig 5shows a single H-bridge which can output three discreet voltage levels. The switches S1and S2are turned –on output voltage is +Vdc ; when switches S3and S4is turned on the output voltage is −Vdc ; when either pair S1 and S3 or S2and S4 is turned on the output voltage is zero.

Generation of Level	Switching States						Output Voltage (Van)
	S1	S2	S3	S4	S5	S6	
2	OFF	ON	ON	OFF	OFF	OFF	2Vdc
1	OFF	OFF	ON	OFF	OFF	ON	1Vdc
0	OFF	ON	OFF	ON	OFF	OFF	0Vdc
-1	OFF	OFF	OFF	ON	ON	OFF	-1Vdc
-2	ON	OFF	OFF	ON	OFF	OFF	-2Vdc

3.Five-Level Switched Capacitor Topology The basic structure of the 5-level topology consists of two H-bridges. One of the H-bridge is connected to an input DC source. The neutral point of both the H-bridge is connected via a bidirectional voltage blocking switch. This5-level inverter circuit is able to produce voltage boosting factor/gain of two.

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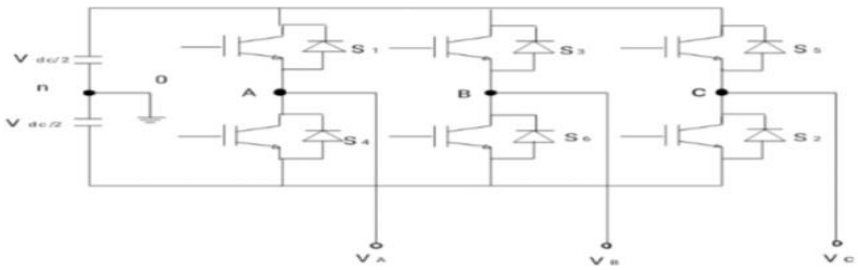

Figure 4.2 Three-Phase Sinusoidal PWM Inverter

Figure 3.1 Single-Phase 5-Level T-Type MLI

4.Definition of modulation Mainly the power electronic converters are functioning in the "switched method". Which means that the switches connected inside the converter are always in either one of the two states - turned off (no current flows), or turned on (immersed with only a small voltage set off downwards across the switch). To control the flow of power in the converter, the switches toggle between these two states (i.e. on and off).
This happens quickly sufficient that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal .The switched component is attenuated and the preferred DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is proscribed by modulating the width of the pulses.

PWM Techniques for Multilevel Inverter: The fundamental methods of pulse-width modulation (PWM) are separated into the traditional voltage-source and current-regulated methods. Voltage-source methods are more easily than current -regulated methods. In separate current-regulated methods the harmonic concert is not as good as that of voltage-source methods. So here we explain only voltage source methods.

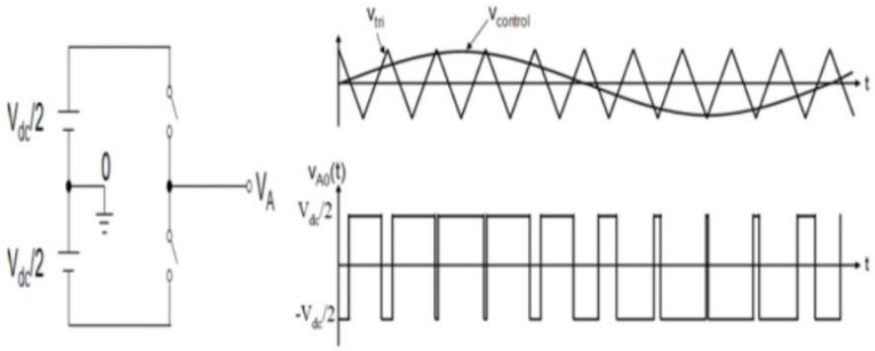

Figure 4.1 Pulse Width Modulation

Where, (VA0)1 is the fundamental frequency component of Va0.

Voltage-source methods:

Voltage-source inverter modulation has taken two major paths; sine triangle modulation in the time domain and space vector modulation in the q-d stationary reference frame. Sine-triangle and space vector modulation are accurately corresponding in every way. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine wave harmonics) is the same to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time).

5.Simulation of 5-level Switched Capacitor Topology: The 5-level switched capacitor MLI is modelled using MATLAB. The MATLAB model for the 5-level MLI. The gate control signals for the switches are obtained from the aggregated waveform using logic circuit.

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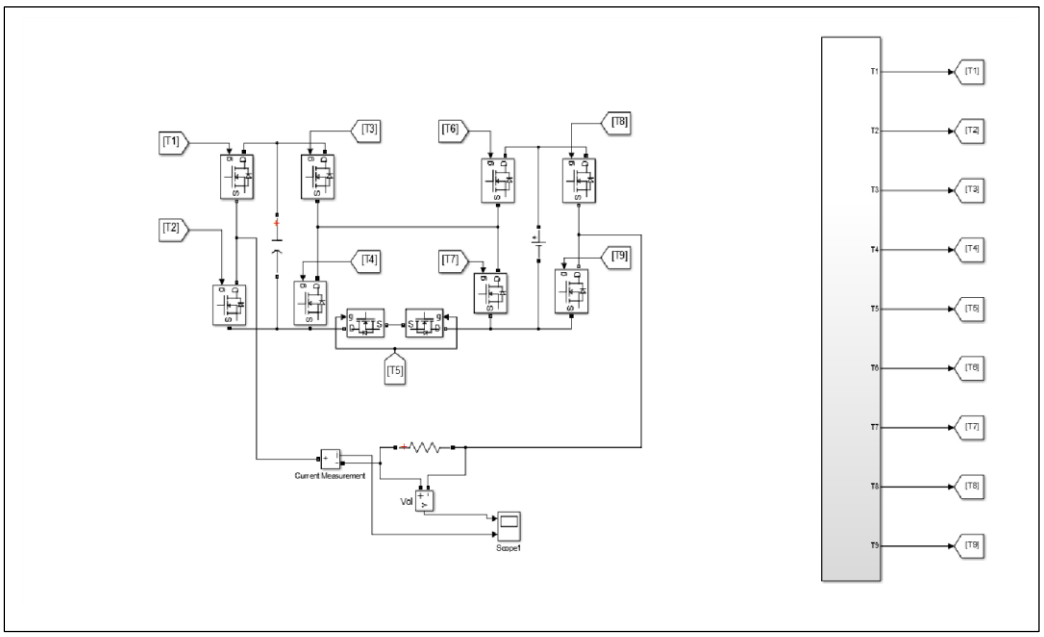

. Fig.8 MATLAB model of 5level SC MLI

6. SIMULATION RESULTS:

The phase voltage of a 5-level MLI. Represents THD at different modulation indexes. It can be observed that there are very few notches in the voltage and current waveforms. For 5-level MLI, corresponding (%) THD PD = 30.57, POD = 31.06, APOD = 31.10, PS = 31.10, ISPWM = 32.27 and VFPWM = 26.77 and SFOPWM = 34.83 at modulation index (Ma) = 0.9 and Mf = 20 are comparative analysis of THD for different PWM techniques is given.

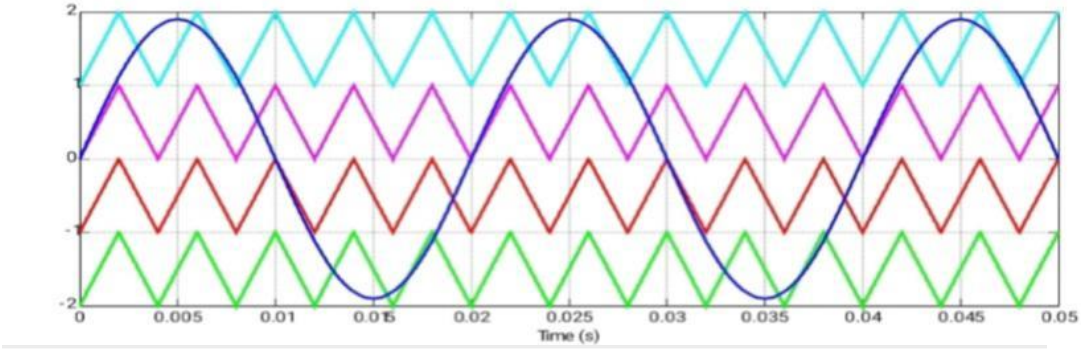

Figure 5.2 Carrier Modulation Signals of Single-Phase 5-Level MLI

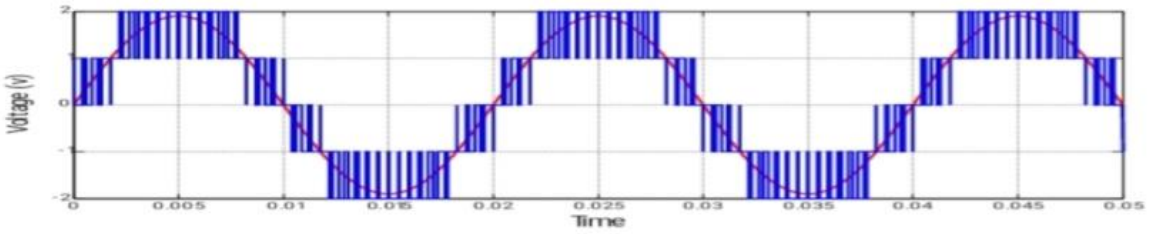

Figure 5.3 Output Phase Voltage of 5-Level MLI for R-L Load.

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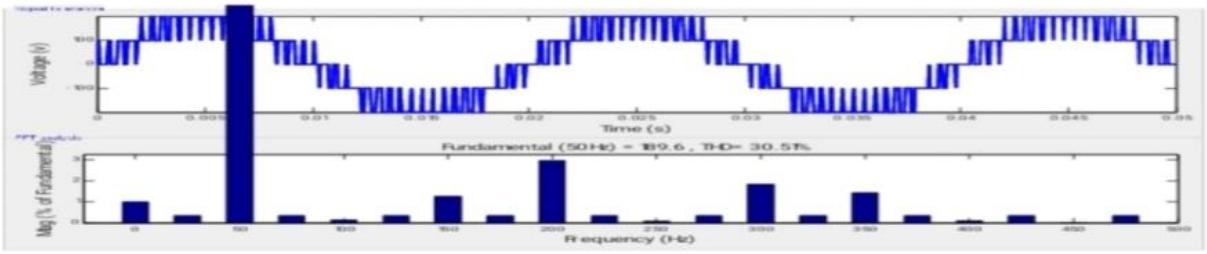

Figure 5.4 Phase Output Voltage by PDPWM for R-L Load (Ma=0.9, Mf=20)

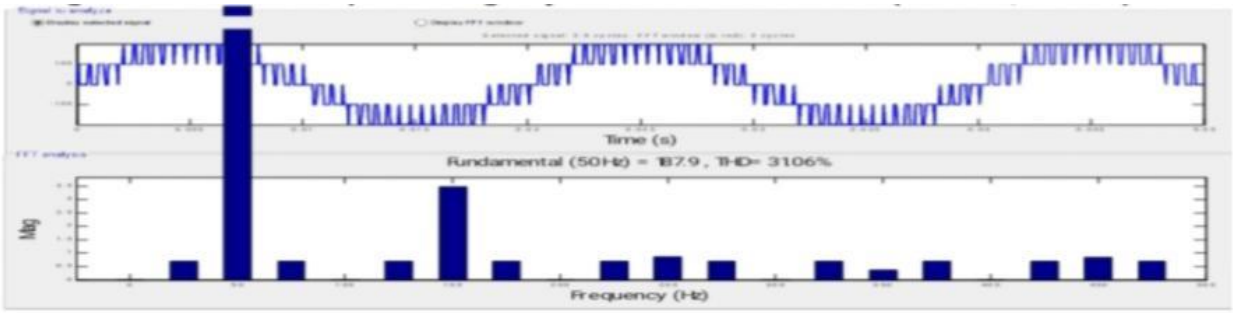

Figure 5.5 Phase Output Voltage by PODPWM for R-L Load (Ma=0.9, Mf=20)

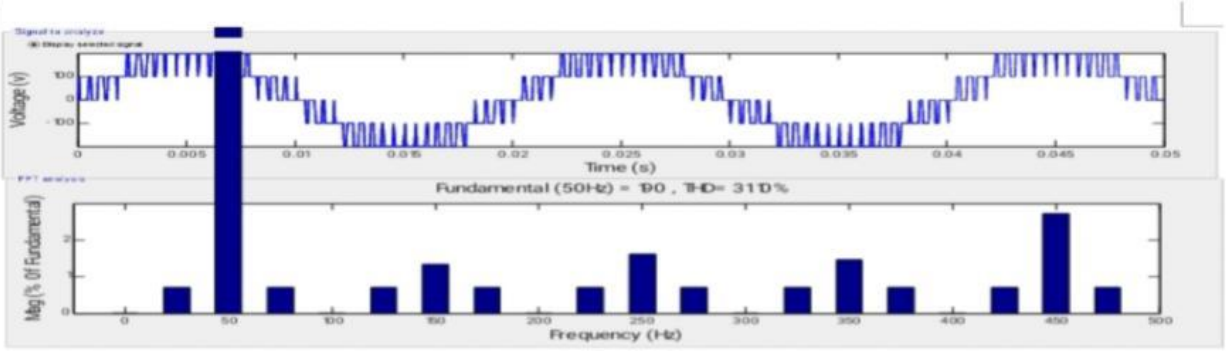

Figure 5.6 Phase Output Voltage by APODPWM for R-L Load (Ma=0.9, Mf=20)

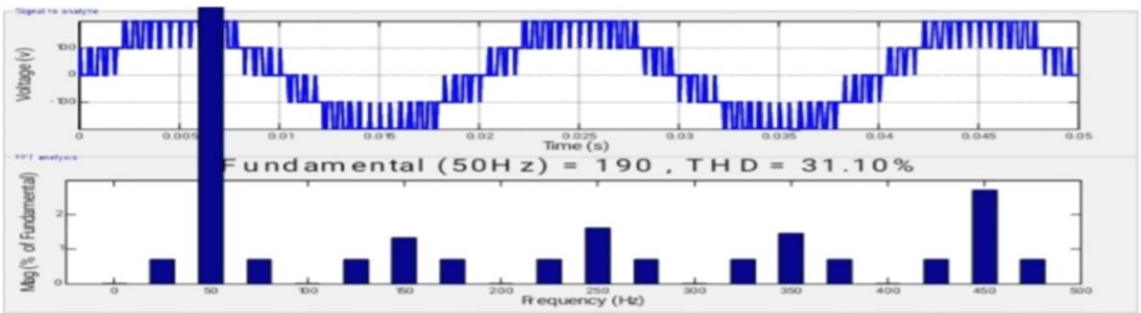

Figure 5.7 Phase Output Voltage by PSPWM for R-L Load (Ma=0.9, Mf=20)

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Modulation Index	PDPWM %THD	POD PWM %THD	APOD PWM %THD	PS PWM %THD
1	28.58	28.32	28.87	29.15
0.9	30.51	31.06	31.10	31.10
0.8	34.70	35.16	34.56	34.56
0.7	36.60	35.53	35.75	35.75
0.6	39.43	38.38	39.27	39.27

7. CONCLUSION

This dissertation has gives a brief summary of proposed MLI circuit topology (5-level, 7-level and 9-level) and their analysis with different PWM techniques.

The simulation results for 5-level, 7-level and 9-level with T-type topology are presented in this dissertation. Their harmonic analysis carried out by using MATLAB R2013a software version. THD values of this MLI have been calculated at different modulation index. Simulation results show the performance of single-phase 5-level, 7-level 9-level MLI with different PWM techniques.

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