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TOPIC MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF POWER ELECTRONICS COMPONENTS

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Abstract: In this paper a " Reduction of THD by Increasing the Levels of Reversing Voltage Multilevel Inverter Using PWM Techniques " is proposed. Because The Conventional Multilevel Inverters (MLI) required big wide variety of Capacitor, Diodes, input sources, electricity switches. So to reduce or overcome from this drawback MLI is used. In this paper an overview of a new multilevel inverter topology named reversing voltage is used. A Single phase 7-level topology is used to reduce the THD. This topology requires less number of components & less gate driver circuits as compared to conventional multilevel inverter topologies and avoids voltage balancing problems

Keywords: MLI Simulation, Modulation Techniques, THD Comparison b/w No. of Components of Conventional & Proposed MLI.

I. INTRODUCTION

Now-a-days power electronic converters with improvement in range are used in industry because they provide reduced energy consumption, high efficiency, better maintenance, improved power quality and so on. Multilevel power structure mainly developed for high voltage and medium voltage conditions alternative to conventional inverter. The term multilevel began with three-level inverter and there after number of multilevel inverter has been developed. However, the multilevel inverters are the modifications of 2-level inverter by connecting number of series small voltages at input and converts into higher voltages at output. Thus the multilevel inverters are used in high voltage and high power applications. The main advantages of multilevel inverter on conventional inverters are that low switching loss, reduction in %THD, low electromagnetic interference, low voltage stress etc.

The multilevel converters are used in traction, high voltage dc transmission, voltage enhancement, VAR compensation, and recently for medium voltage induction motor variable speed drives. Many multilevel convertors mainly focus on medium voltage industrial drives, traction drive system and flexible ac transmission.

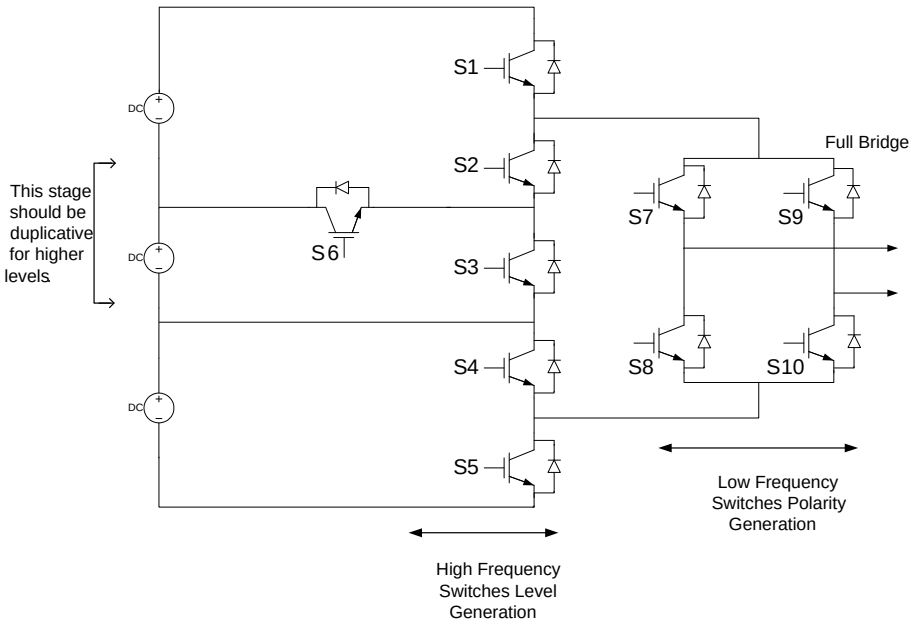

Fig. 1 Multi-level inverter using Reversing Voltage topology.

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The block diagram of multi-level inverter using Reversing Voltage topology is shown in Fig. 1 In this figure, the left side circuit (i.e., positive level generator) generates the required positive level is called positive level generator and the right side circuit is called full bridge converter which reverses the voltage direction when the voltage polarity requires to be changed for negative polarity (negative half cycle of the fundamental output voltage). This topology requires less number of components & less gate driver circuits as compared to conventional multilevel inverter topologies and avoids voltage balancing problems. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. This topology is also required lower (%) THD in comparison of other MLI topologies. The main advantage of this topology is to control the EMI, minimize the total harmonic distortion with different PWM techniques using Reversing Voltage topology and it also minimizes power semiconductor switches than conventional multilevel inverter.

II. MODULATION TECHNIQUES

There are numerous modulation techniques for multi-stage inverters. Multilevel inverter has to synthesize a sinusoidal waveform by using the modulation technique to get the controlled output voltage.

- **PD PWM:** Phase disposition PWM has carriers in same phase above and below zero reference line. All the carriers are in same phase in this method of PWM. Most widely used method as it provides load voltage and current with lower harmonic distortion
- **POD PWM:** Unlike the phase disposition this method has all carriers at the same frequency with adjustable amplitudes. The only difference that it has when compared to the above method is that it has carriers above zero level reference in phase among them but in opposition usually 180 degrees phase shifted with those of below
- **APOD PWM:** This method of multicarrier pulse width modulation is quite different from the above two which has all the carriers alternately in opposite disposition
- **PS PWM:** PS-PWM is generally preferred for cascaded multilevel inverters as it ensures equal power distribution and equal switching frequency on all the switches within a given module. This technique however suffers from lack of optimal switching.

III. 7-LEVEL REVERSING VOLTAGE MLI

This proposed RV topology for 7-level MLI requires ten semiconductor switches and three isolated dc sources shown in Fig.1 which separates output voltage in two parts. This topology combines the two parts to generate the multi-level output voltage waveform. The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. This RV multilevel inverter easily extends to higher voltage levels by increasing the middle section as shown in Fig. 1. It can also be applied for three-phase applications with the same principle.
Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. In Fig.2 the complete 3-phase MLI for 7-level is shown. For a conventional single-phase 7-level inverter model, it uses 12 switches, whereas the proposed model uses only 10 switches and for three-phase 7-level inverter model, it uses 36 switches, whereas the proposed model uses only 30 switches.

IV. OPERATION OF 7-LEVEL REVERSING VOLTAGE MLI

Operation of the single-phase 7-level Reversing Voltage topology can be easily explained with the help of Fig.1 and switching table 1. When switches S2, S4, S6, S8 and S9 are turned “on” the output voltage will be “V_{dc}” (i.e., level 1). The output voltage will be “$2V_{dc}$” (i.e., level 2) when switches S1, S4, S8 and S9 are turned “on. When S1, S5, S8 and S9 switches are turned “on” the output voltage will be “$3V_{dc}$” (i.e., level 3). When switches S2, S3, S4, S7 and S10 are turned “on” the output voltage is zero (i.e., level 0). Switches S9, S10, S11 and S12 are used for a complementary pair. When S8 and S9 are turned “on” together, positive half cycle (level +1, level +2, level +3) can be generated and when S7 and S10 are turned “on” together, negative half cycle (level -1, level -2, level -3) can be generated across load. The voltage blocking capacity of each switch is $V_{dc.}$.

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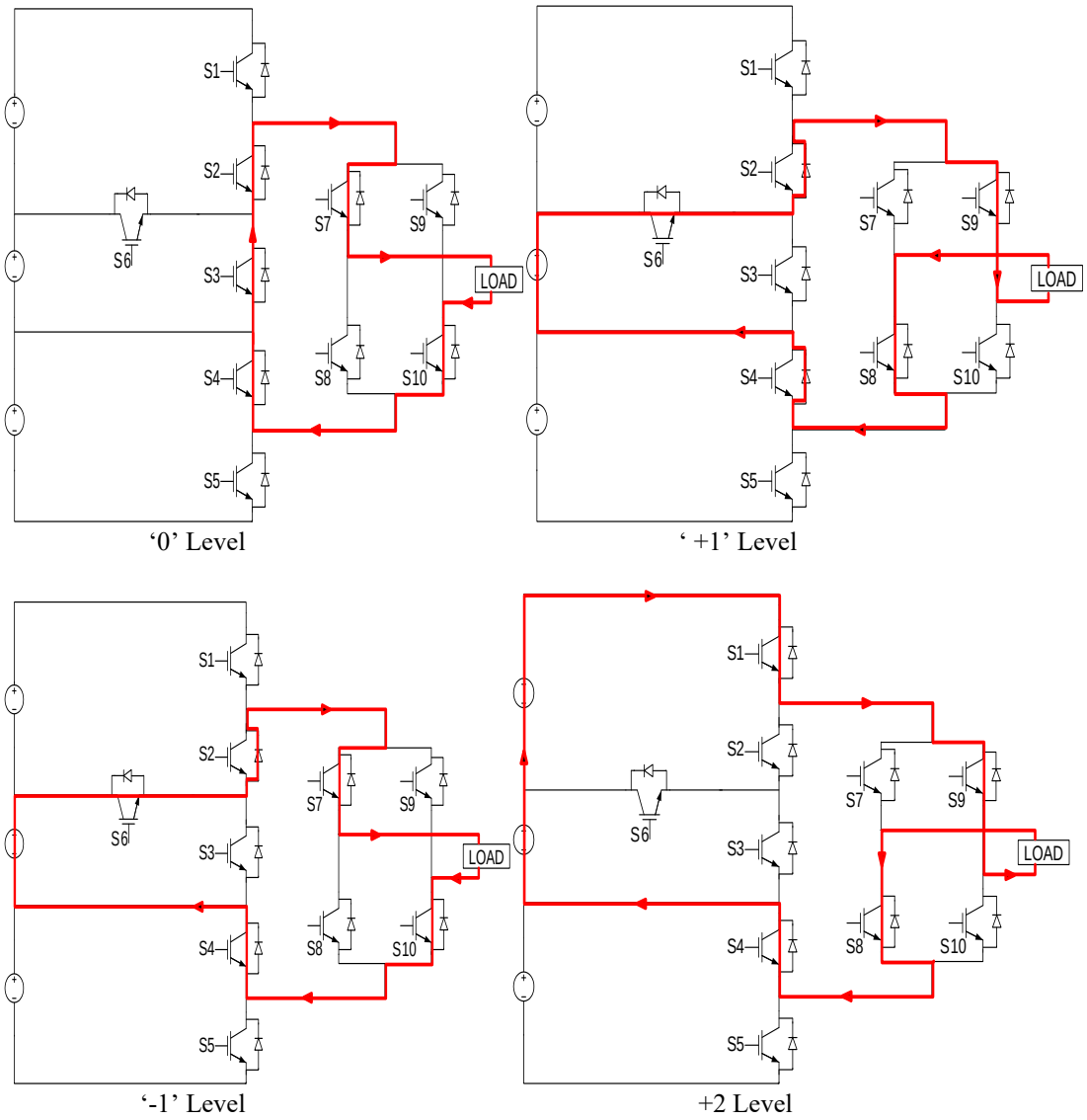
MODES OF OPERATION



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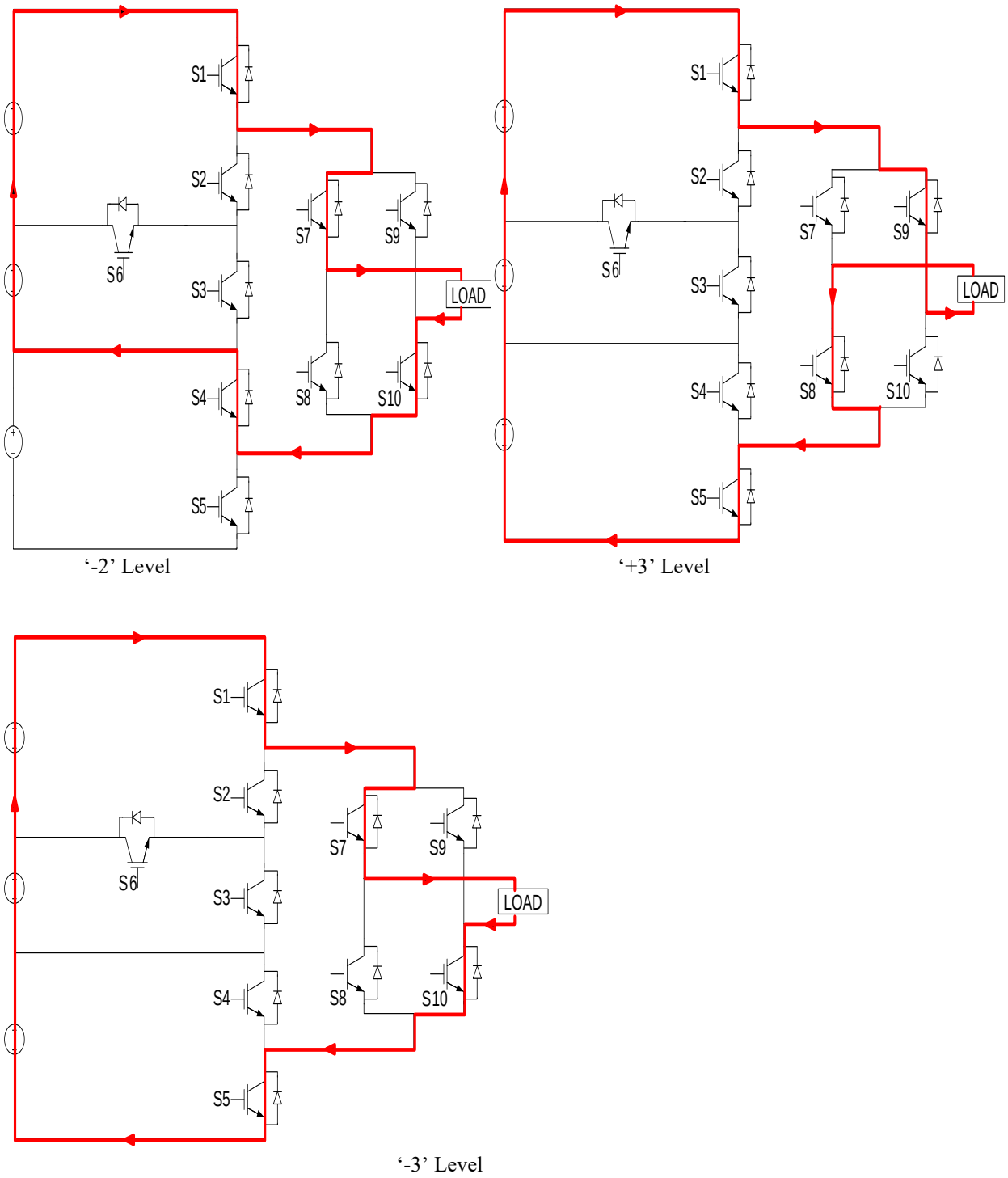

Fig. 2 Shows the modes of operation of 7-level reversing voltage multilevel inverter.

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Table I : Switching Table of 7-level RVMLI

LEVEL	SWITCHING STATES										OUTPUT VOLTAGE
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*	*S10*	
3	ON				ON			ON	ON		3Vdc
2	ON			ON				ON	ON		2Vdc
1		ON		ON		ON		ON	ON		Vdc
0		ON	ON	ON			ON			ON	0
-1		ON		ON		ON	ON			ON	-Vdc
-2	ON			ON			ON			ON	-2Vdc
-3	ON				ON		ON			ON	-3Vdc

TABLE II : Comparison b/w No. of Components of Conventional & Proposed MLI

Inverter / Components	DC MLI	CHB MLI	FC MLI	Reversing Voltage MLI
Switches	6(N-1) = 72	6(N-1) = 72	6(N-1) = 72	3((N-1)+4) = 48
Diodes	6(N-1) = 72	6(N-1) = 72	6(N-1) = 72	3((N-1)+4) = 48
Clamping Diodes	3(N-2)(N-1) = 396	-	-	-
DC supply	(N-1) = 12	3(N-1)/2 = 18	(N-1) = 12	(N-1)/2
Flying Capacitor	-	-	3(N-1)(N-2)/2 = 198	-

V. SIMULATION MODEL & RESULT OF REVERSING VOLTAGE MULTILEVEL INVERTER

Simulation

In this section a model of proposed topology for a single-phase 7-level MLI is implemented. The simulation parameters are as following R = 10 ohms, L = 10mH, dc source voltage is 100V for each V_{dc}, frequency of carrier signal is 1 kHz. In this paper, four PWM techniques are used PD PWM, POD PWM, APOD PWM, PS PWM, with different modulation index (M_a). Based on the PWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink R2009a software version.

7-Level Reversing Voltage MLI

In 7-level MLI is model we are taking six carrier signals. Three of them are applied across the positive half cycle of the modulating signal. Remaining three of them is applied across the negative half cycle of the modulating signal. From these signals ten PWM pulses are generated and theses pulses are given to the switches in one phase leg of a 7-level MLI. Similarly the pulses are generated for next two phases. The only difference is that the modulating signal is phase shifted by 120 degrees. Fig.3 shows the simulation model of a 7-level single-phase MLI.

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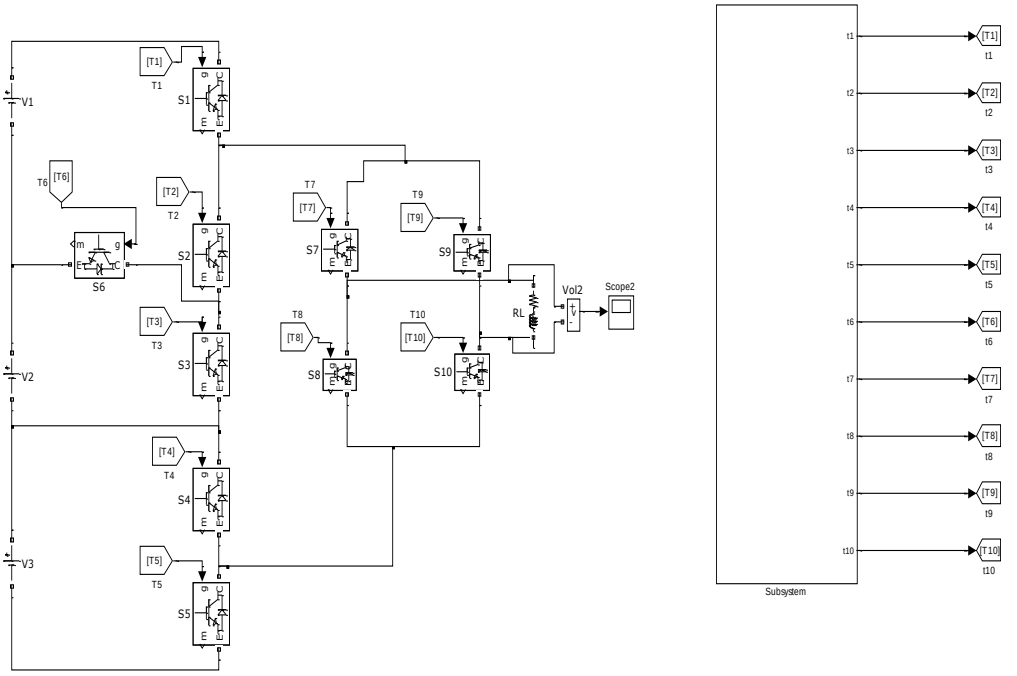

Fig. 3 Simulation Model of 7-Level RVMLI

Simulation Result

Fig.4 shows the phase voltage of a 7-level MLI. Table VI represents THD at different modulation indices. It can be observed that there are very few notches in the voltage and current waveforms. For 7-level MLI, corresponding (%) THD PS = 18.67, PD = 18.62, POD = 18.98, APOD = 18.49, PS = 22.03, at modulation index (M_a) = 1.0 and M_f = 20 are shown in Fig.4 to Fig. 8. Comparative analysis of THD for different PWM techniques is given in Table. III

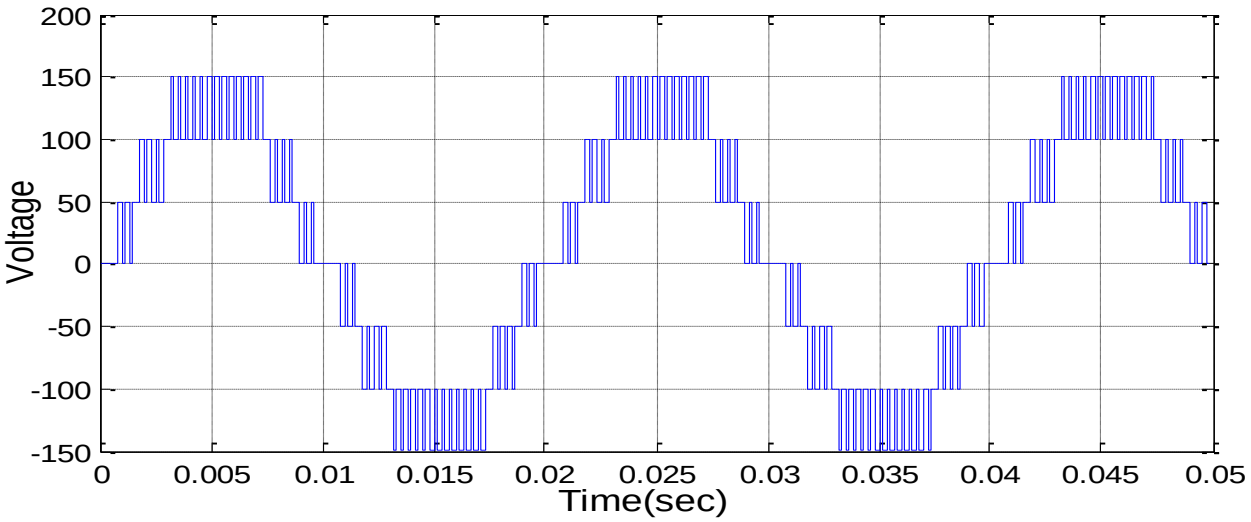

Fig. 4 Phase Voltage of a 7-level MLI for R-L Load

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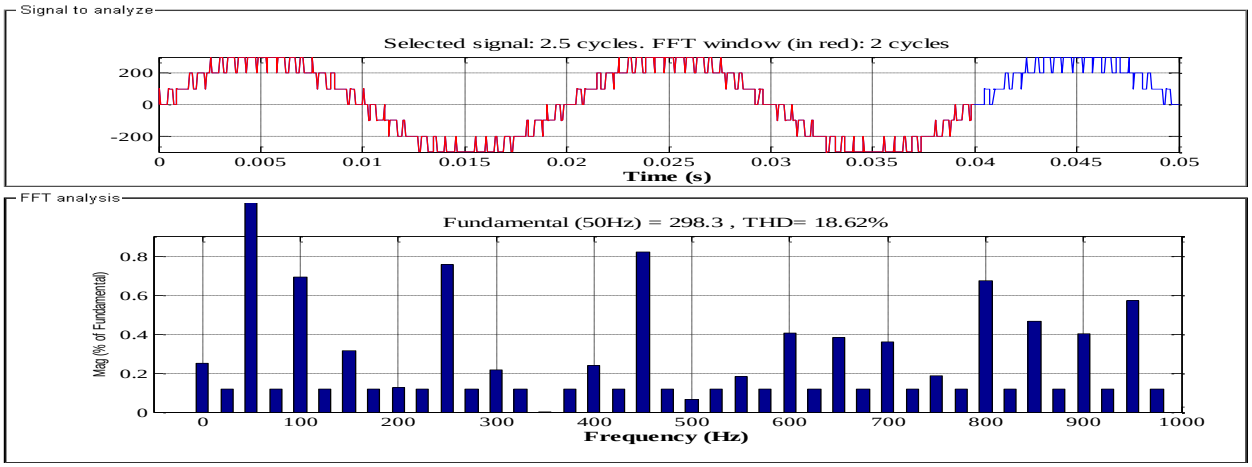

Fig. 5 Phase output voltage by PDPWM for R-L load

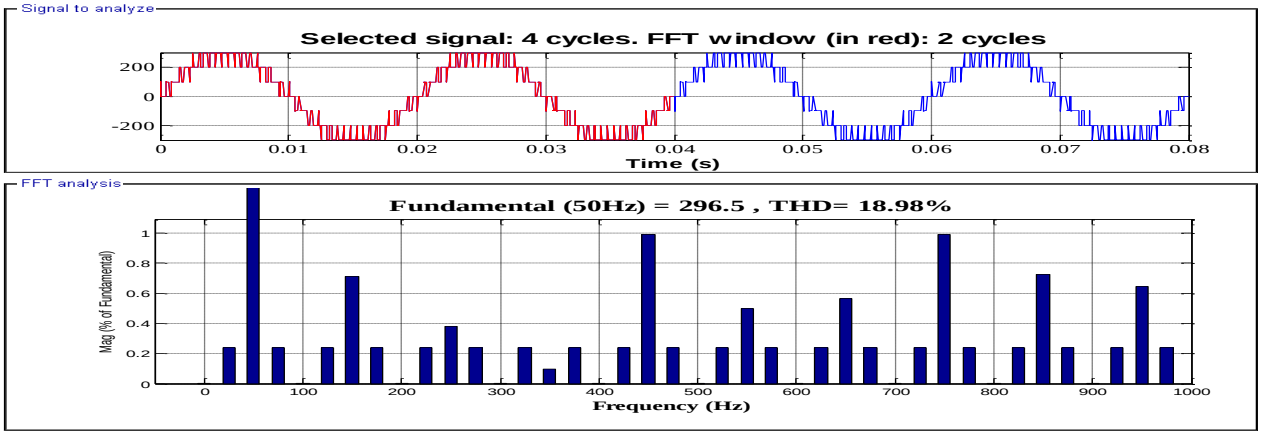

Fig. 6 Phase output voltage by PODPWM

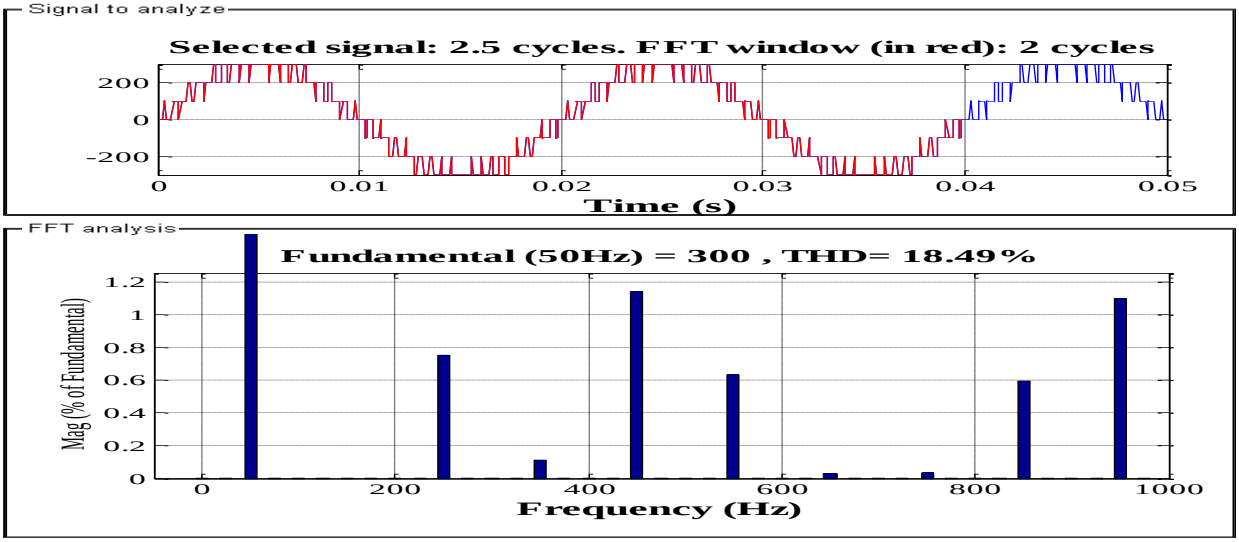

Fig. 7 Phase output voltage by APODPWM

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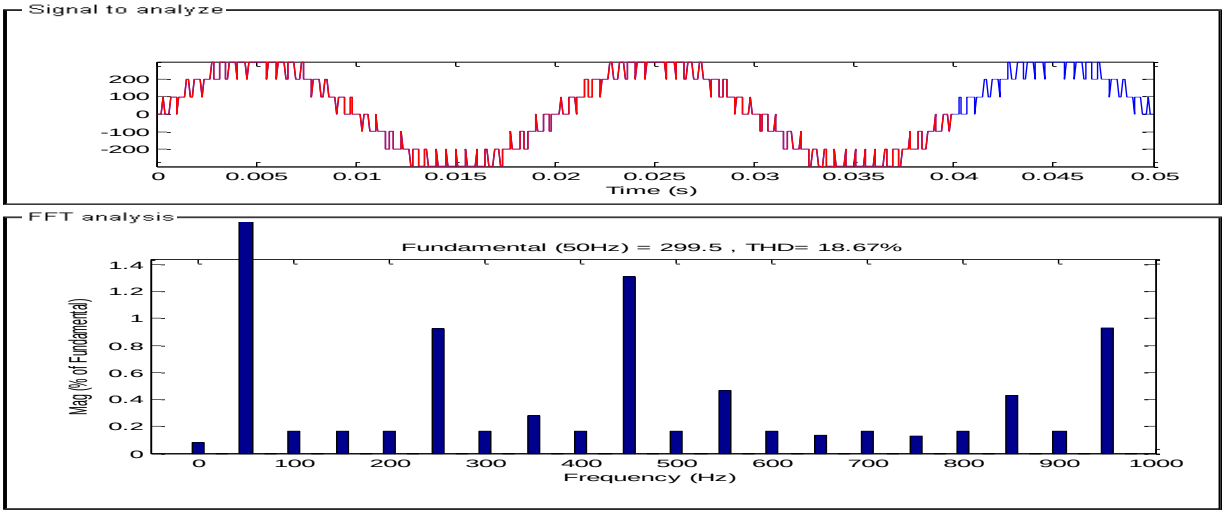

Fig. 8 Phase output voltage by PS PWM

TABLE III : Comparative[8] THD analysis of different PWM techniques for 7-level MLI

Modulation Index	POD PWM %THD	PD PWM %THD	APOD PWM %THD	PS PWM %THD
1	18.98	18.62	18.49	18.67
0.9	19.48	19.72	19.96	19.96
0.8	21.73	22.27	21.91	23.79

VI. CONCLUSION

Reduction of THD achieved by Increasing the Levels of Reverse Voltage Multilevel Inverter Using PWM Technique simulated using MATLAB R2009a. The simulation results for 7-level with RV topology are presented in this thesis. Their harmonic analysis carried out by using MATLAB R2009a software version. THD values of this MLI have been calculated at different modulation index. Simulation results show the performance of single-phase and three-phase 7-level, 9-level, 11-level and 13-level MLI with different PWM techniques.

FUTURE WORK

In this dissertation work proposed a 7-level proposed MLI topology in single phase. With the help of proposed MLI topology we will increase the voltage levels with less number of power switches, capacitors and diodes and compare with the DCMLI, CHBMLI and FCMLI. In future it is being proposed that the same MLI topology will fed with the induction motor drives using direct torque control.

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