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Implementation of Seven-level Asymmetrical Cascaded H-bridge Inverter Using PIC16F877A Microcontroller

Shivacharan Nayak[1], Sujatha Balaraman[2]

PG-Scholar, Department of Electrical Engineering, Government College of Technology, Coimbatore, India [1]

Associate Professor, Department of Electrical Engineering, Government College of Technology, Coimbatore, India [2]

Abstract: Industrialisation is the transformation of agrarian society into an industrial society. Historically it is associated with growth in industries heavily dependent on fossil fuels which were often polluting; however, with the increasing focus on sustainable development most of the industries are looking for cleaner and renewable technologies. With an upward surge of power requirement, the demand for efficient inverters is pullulating as well. In this paper, asymmetrical cascaded multilevel H-bridge inverter (CHB MLI), one of the popular inverters is recced for its better output power quality, low power loss and implementation complexity, economic feasibility and relative advantages. A seven-level asymmetrical CHB MLI is used to improvise the output voltage spectrum. For the purpose, initially the system is tested in MATLAB/Simulink, then pulses are generated through pulses width modulation (PWM) technique using microcontroller and finally implemented in hardware after design and testing in Proteus ISIS. The hardware setups use MOSFETs as switching devices and low-cost PIC microcontrollers for generating the switching pulses via level shifted in-phase disposition pulse width modulation. Ultimately, the hardware outputs are verified with simulation results.

Keywords: PWM techniques, MOSFET, Inverter, Multilevel Inverter (MLI), PIC16F877A, Asymmetrical Cascaded Multilevel H-bridge inverter (CHB MLI)

I. INTRODUCTION

Power is one of the essential factors of infrastructure, economic growth and welfare of any nation. The judicious development of industrial infrastructure plays a vital role in national economy [1]. India's power sector is greatly dispersed and diversified in the world. Power generation sources range from conventional sources such as coal, natural gas, fossil fuels and nuclear power to viable renewable sources such as wind energy, solar panels and biofuel. With increment in urbanization in this digitized world, the demand for power consumption is vast. By 2022, it is estimated that power extraction from various non-conventional sources would be around 230GW [2]. In this ongoing revolution, solar photovoltaic (PV) power networks play a huge part. But PV systems require efficient devices for conversion of direct current in order to meet proper handling of transmission and distribution system. A power inverter is a power electronic device harnessed for turning DC to AC. Power inverters are primarily used in electrical power applications where high currents and voltages are present [3].

The cascaded H-bridge multilevel inverter is a topology which contains series of power conversion cells so that power can be easily ascended. The combination of capacitors and switch pairs is called an H-bridge. Each H-bridge requires a separate input DC voltage. Each cell of an H-bridge can provide the three different voltages like zero, positive DC, and negative DC voltages [4] [5]. One of the greatest advantages CHB MLI is that it needs comparatively lesser number of components than diode clamped and flying capacitor multilevel inverters. Multilevel cascaded inverters are used to eliminate the usage of heavy transformer in conventional multi-phase inverters. In case of diode clamped inverters, clamping diodes required and flying capacitors are must in flying capacitor inverters whereas this type of inverter needs just a large number of isolated voltages to supply each cell. The multilevel converter is widely used for its several attributes such as common-mode voltage to reduce overall stress on motor, input current with low distortion, operation at both higher and lower switching frequencies and limited total harmonic distortion in the output waveform without using any filter circuit [5]. Asymmetrical Cascaded H-Bridge Multilevel Inverter: DC sources are broadly classified into two types- Asymmetrical DC source and symmetrical DC source. Asymmetrical DC source has unequal magnitude of voltage whereas Symmetrical DC source has equal magnitude of applied voltage. When an asymmetrical DC source is supplied to a CHB MLI, it is called an asymmetrical cascaded H-bridge multilevel inverter [6]. In this paper, Asymmetrical cascaded MLI has been used for implementation as it has several advantages over symmetrical cascaded MLI for an instance, A-CHB MLI requires a smaller number of DC source voltage and switches, increased number of voltage levels for a given module counts and so on.

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II. SIMULATION OF SEVEN-LEVEL ASYMMETRICAL MULTILEVEL INVERTER

In this section various simulations, waveforms are obtained to understand the performance of seven-level ACHB. Apart from this FFT analysis are carried out in order to understand the harmonic spectrum. For this purpose, MATLAB 2019a as a software used for implementation. To implement the model in MATLAB 2019a, Simulink modelling feature has been used. The Asymmetrical cascaded seven level multilevel inverter has two DC sources and eight power switches magnitude of DC sources are V_1 and V_2 respectively [7]. The sources are connected to two H-Bridge units which are cascaded in single phase [8]. In an individual H-bridge the output voltage is $+V_{DC}$, 0 or $-V_{DC}$. Hence the desired output voltage for seven level Asymmetrical CMLI are 0, $+3V_{DC}$, $+2V_{DC}$, $+V_{DC}$, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$. In order to get desired output voltage, the power switches are turned ON and OFF in various combinations [9]. For maximum output voltage $+3V_{DC}$; the switches S_{11}, S_{22}, S_{21} and S_{12} are ON and remaining switches are OFF at this time. For $+2V_{DC}$; the switches S_{12}, S_{14}, S_{21} and S_{22} are ON and remaining switches are OFF at this time. For $+V_{DC}$; the switches S_{11}, S_{12}, S_{21} and S_{23} are ON and remaining switches are OFF at this time. Similarly, remaining other voltage levels can be analyzed with the help of following Table I.

Table I: Switching pattern for seven-level ACHB MLI

Levels Switches	$3V_{DC}$	$2V_{DC}$	V_{DC}	0	$-V_{DC}$	$-2V_{DC}$	$-3V_{DC}$
S_{11}	1	0	1	0	0	0	0
S_{12}	1	1	1	0	0	1	0
S_{13}	0	0	0	0	1	0	1
S_{14}	0	1	0	0	1	1	1
S_{21}	1	1	1	0	1	0	0
S_{22}	1	1	0	0	0	0	0
S_{23}	0	0	1	0	1	1	1
S_{24}	0	0	0	0	0	1	1

Modulation methods developed for multilevel inverters involve multilevel sinusoidal pulse width modulation. Multilevel selective harmonic elimination and space-vector modulation. It is generally accepted that the performance of any inverter, with any switching strategy can be related to the harmonic contents of its output voltage. There are many control techniques reported for cascaded multilevel inverter [10]. But the popularly used modulation method is the multicarrier level shifted PWM technique. Level shifted PWM technique is the generally used method in cascaded multilevel inverter as it gives a reduced THD. In this research work, fixed frequency PWM is proposed which uses the conventional sinusoidal reference signal and the carrier signals with variable frequency. To implement a m-level inverter, (m-1) carriers are used [10] [11]. There are six distinct carriers with fixed frequency and with the same magnitudes for the seven-level multilevel inverter ; the difference between the carriers is that they are all displaced by a set of DC offset. The frequency modulation index is given by

$$m_f = \frac{f_c}{f_m} \tag{1}$$

$$m_a = \frac{V_m}{V_{cr(m-1)}} \qquad for\ 0 \le m_a \le 1 \tag{2}$$

$$f_{sw} = f_c \tag{3}$$

where,

m_f = modulation index, f_c = carrier frequency, f_m = modulating waveform frequency, m_a = amplitude modulation index V_m = peak value of the modulating waveform, V_{cr} =peak value of the carrier waveform, f_{sw} = switching frequency of inverter using level-shifted modulation

The following figures shows the simulated waveforms for a seven-level inverter operating under the condition of $m_f = 57$, $m_a = 1.0$, $f_m = 50$ Hz, and $f_{cr} = 2850$ Hz. Although the carrier frequency of 2850 Hz seems high for high-power converters, the average device switching frequency is only 712 Hz. Fig. 1 shows three schemes for the level-shifted multicarrier modulation:(a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference [11] [12].

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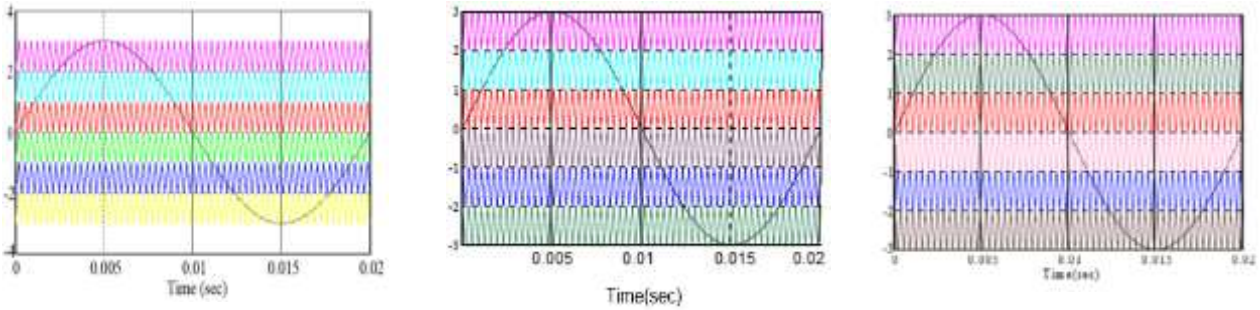

(a) (b) (c)

Fig. 1 Reference and carrier waveform for (a) PD CLSPWM (b) APOD CLSPWM (c) POD CLSPWM

For seven-level asymmetrical cascaded multilevel inverter driver by phase shifted carrier, six phase shifted carrier waves are required and the phase shift between two consecutive carriers is 90 degrees as shown in fig. 2

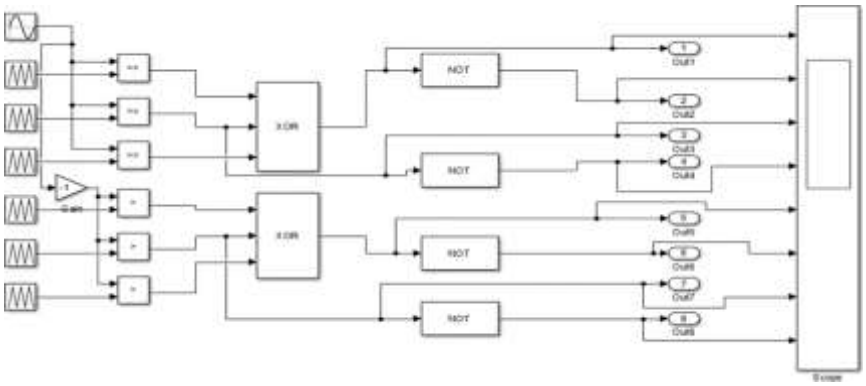

Fig. 2 Control circuit of seven-level asymmetrical multilevel inverter

The performance analysis has been carried out for seven-level Asymmetrical inverters with resistive load using following parameters specified in Table II**.**

Table II Various input parameters for seven-level Asymmetrical MLI

Parameter	**Value**
Voltage	36 V
V_1	12 V
V_2	24 V
Frequency	50 Hz
Load(R)	1000Ω

The complete result is observed in MATLAB/SIMULINK .The complete simulation circuit for Asymmetrical seven-level MLI with resistive load are shown in Fig. 3

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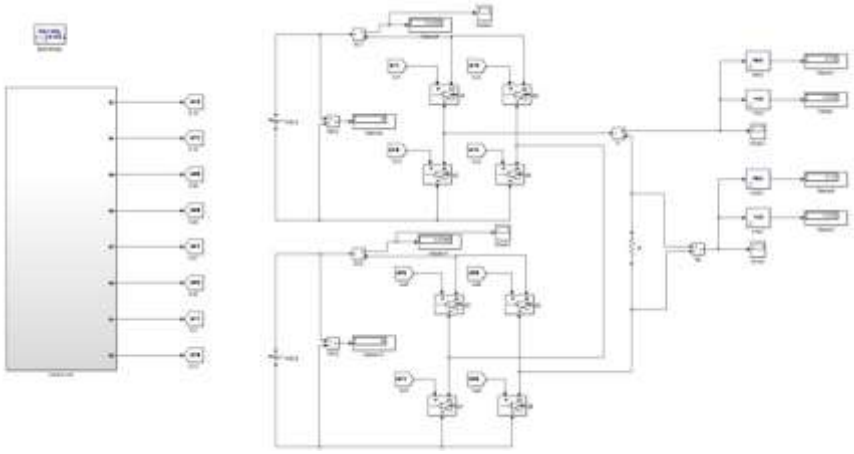

Fig. 3 Simulink model for seven-level Asymmetrical MLI

III. RESULTS AND DISCUSSIONS

In this section various output waveforms with its FFT has been discussed to understand the performance of the seven-level asymmetrical multilevel inverter. It has been found that the model procures 60.33 V as its peak-peak line voltage, 0.06033 A as its peak-peak line current and 21.21% voltage and current THD with 8 number of switches. The output voltage waveform of seven-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 4.

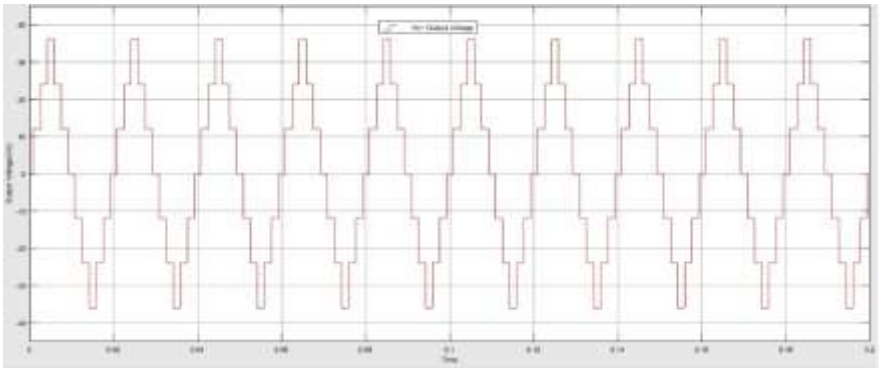

Fig.4 Output Voltage waveform for 7-Level Asymmetrical Multilevel Inverter

The output current waveform of seven-level Asymmetrical cascaded MLI with resistive load is shown in Fig. 5.

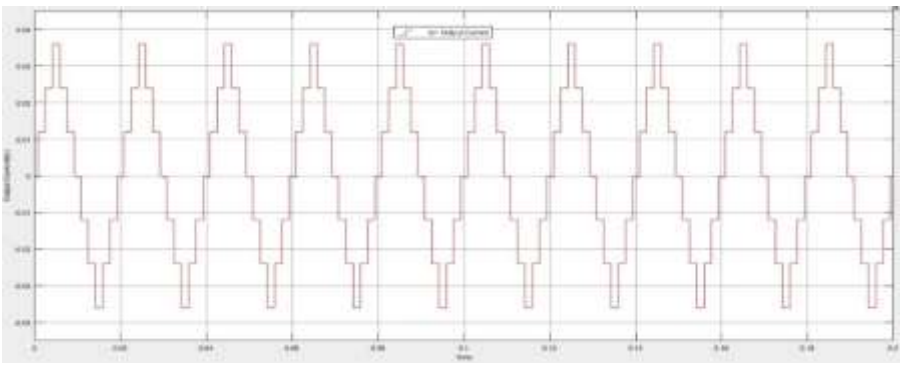

Fig. 5 Output Current waveform for 7-Level Asymmetrical Multilevel Inverter

Fig. 6 illustrates the FFT window and its respective FFT analysis of voltage. As per the spectrum, the seven-level asymmetrical multilevel inverter results THD of 21.21% for voltage with resistive load

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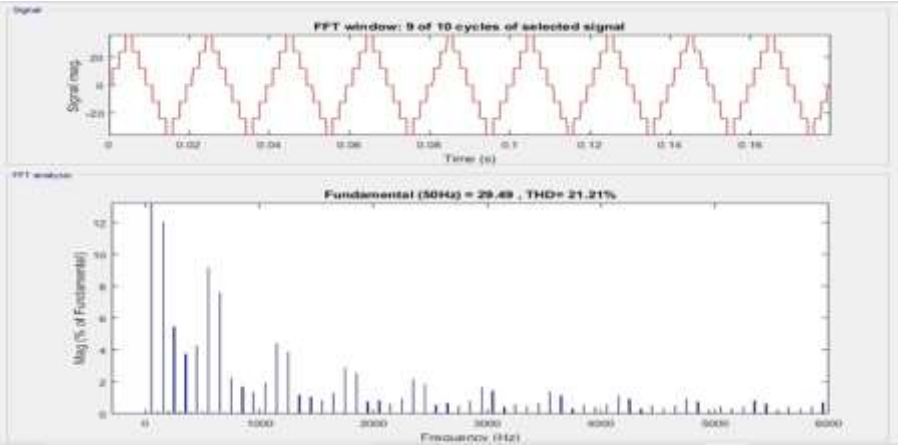

Fig. 6 FFT Analysis of voltage waveform of 7-Level Asymmetrical Multilevel Inverter

Fig. 7 illustrates the FFT window and its respective FFT analysis of current. As per the spectrum, the seven-level asymmetrical multilevel inverter results THD of 21.21% for current with resistive load

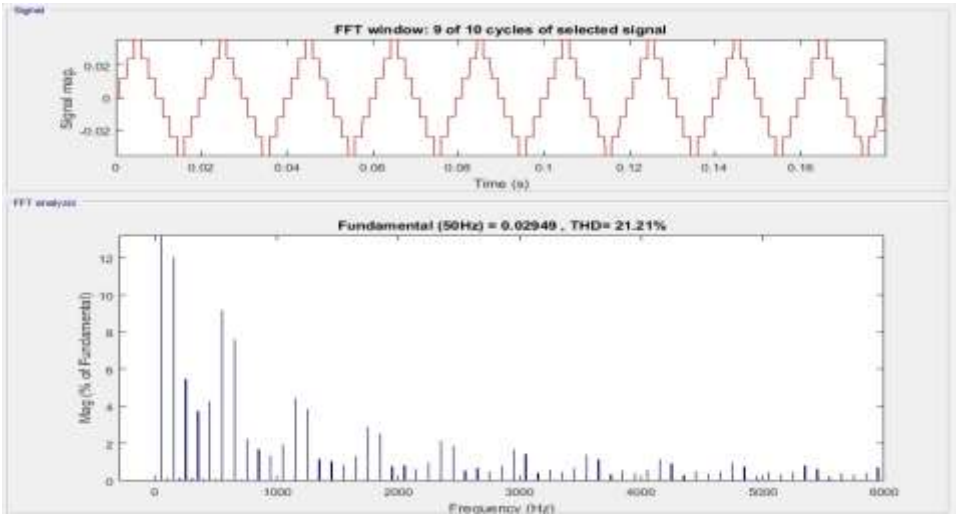

Fig. 7 FFT Analysis of current waveform of 7-Level Asymmetrical Multilevel Inverter

This section elucidates detailed description of components deployed in hardware, working mechanism of hardware implementation and finally the results in form of a comparison analysis of values obtained from MATLAB/Simulink and experimental setup. The block diagram picturizes how the various components of the model are connected to make up the complete circuit of the hardware. Initially, power supply is distributed to voltage regulator and driver unit. Through the controller, voltage regulator is connected to the driver unit. The driver unit is directly applied to the inverter. Batteries supply power to the inverter. Lastly, the output is measured across the load.

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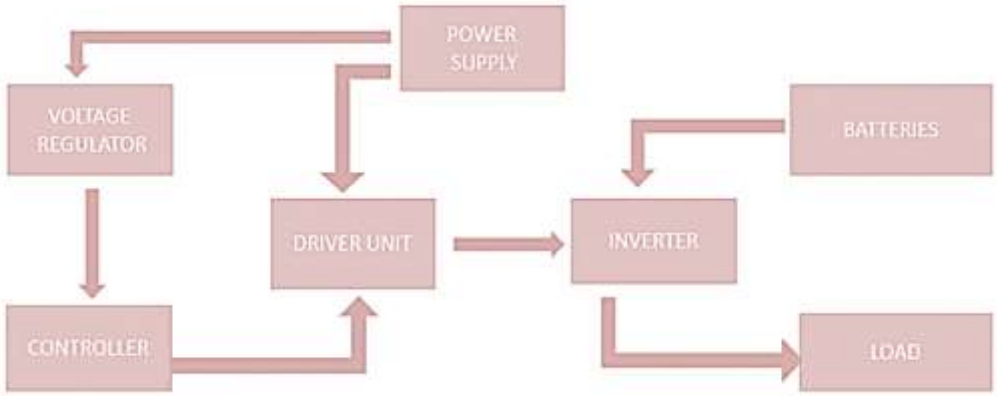

Fig. 8 Block diagram for hardware implementation

PIC 16F877A is used for producing switching pulses to multilevel inverter. so as to use those vectors which do not generate any common mode voltage at the inverter poles. .This eliminates common mode voltage. Also, it is used to eliminate capacitor voltage unbalancing. The microcontroller is driven via the driver circuit so as to boost the voltage triggering signal to 9 V. To avoid any damage to micro controller due to direct passing of 230 V supply to it, an isolator is provided in the form of optocoupler in the same driver circuit.

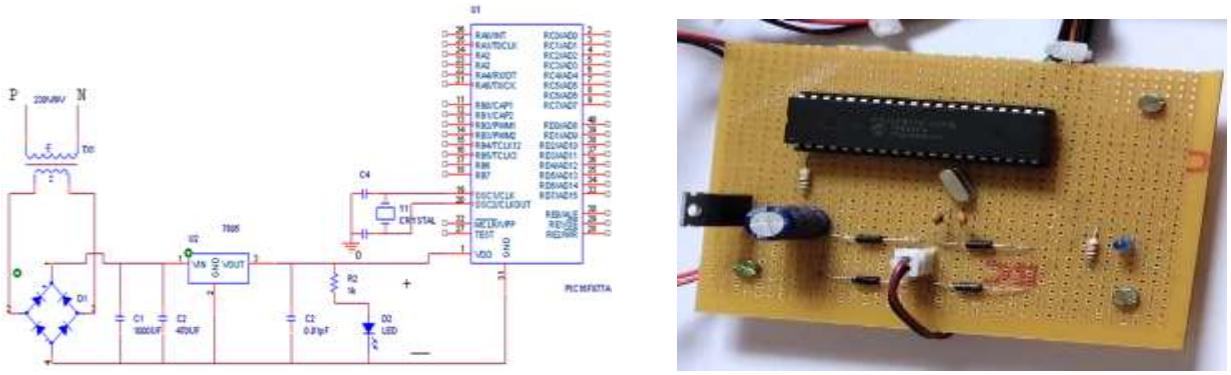

Fig. 9 Triggering circuit

There are totally six transformers, three of them are input transformers and remaining are power transformers . The input transformers are connected to a driver circuit and a PIC microcontroller. Driver circuit requires DC power thus full wave rectifiers are employed in order to get DC from AC provided by transformers. The rectified DC is pulsating in nature so capacitors are used to filter out AC components from the supply. This conditioned DC is fed to the driver circuit. PIC microcontroller needs constant voltage of about 5-12 V hence it is connected to input transformer. With the help of a Dumping Kit, requisite program is applied to the PIC microcontroller which in return generates pulses through PWM technique. Now these pulses are supplied back to the driver circuit. Then the driver circuit amplifies the given pulses such that the amplification so produced is sufficient enough to turn the gate switches of the main circuit ON. The driver circuit also acts as an optocoupler which segregates input and main circuits. The power transformers produce 12 V and 24 V for H_1 and H_2 bridges respectively.

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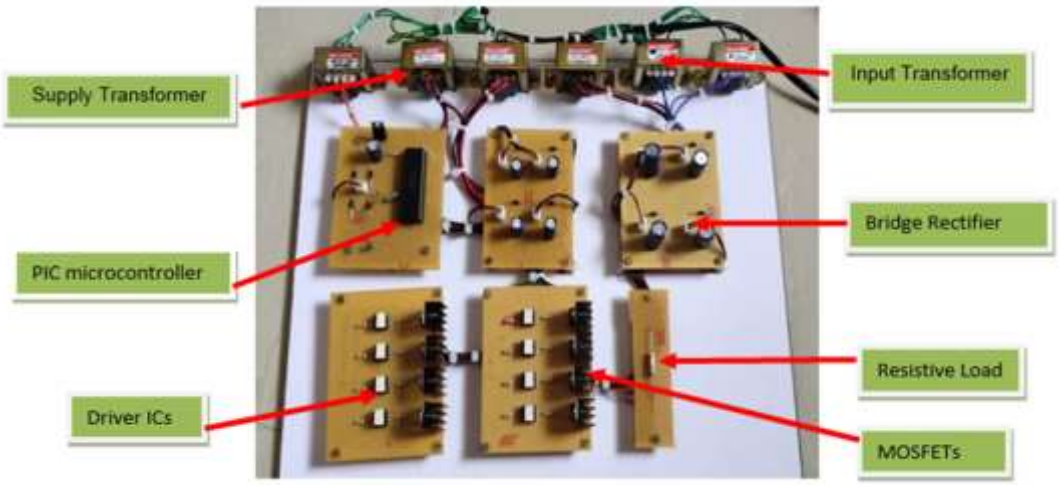

Fig. 10 Hardware setup of seven-level AMLI

Fig. 11 demonstrates the hardware setup in real time. Here, the glowing blue LED affirms the connections are correct and circuit is working properly. At load terminal, the measuring probes of DSO is connected to measure output line voltage. The fig. 12 shows the DSO output of the experimental setup. The scope window displays the peak-peak line voltage and frequency as 59.60 V and 48.36 Hz respectively.

Table III: Hardware components used to implement the seven- level ACHB MLI hardware

Symbol	Name	Rating
S_{11}-S_{24} (8 no.s)	MOSFET (IRF840 2B,3L, R1920P)	500 V, 8.0 A
R_{imp} (16 no.s)	Impedance resistors	22 Ω
R_L	Load resistor	1 k Ω
C_F	Filtering Capacitors	1000µF
O_C (8 no.s)	Optocoupler	TLP250H
M	PIC Microcontroller	PIC16F877A
B_R (2 no.s)	Bridge Rectifier	BR305/35
I_T (3 no.s)	Input Transformer	0-6V, 500 mA
I_p (3 no.s)	Power Transformer	0-12 V, 300mA

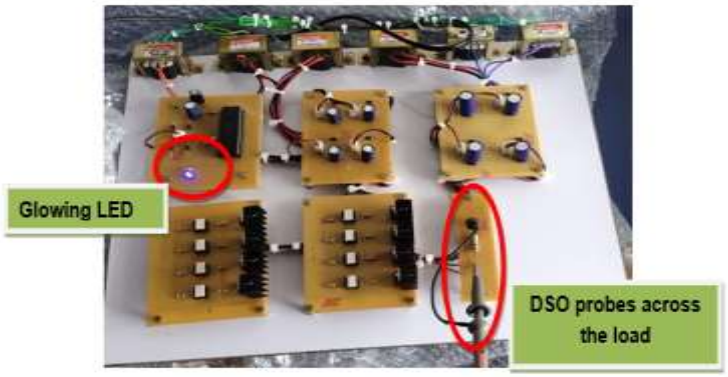

Fig. 11 Real-time Hardware setup of seven-level AMLI

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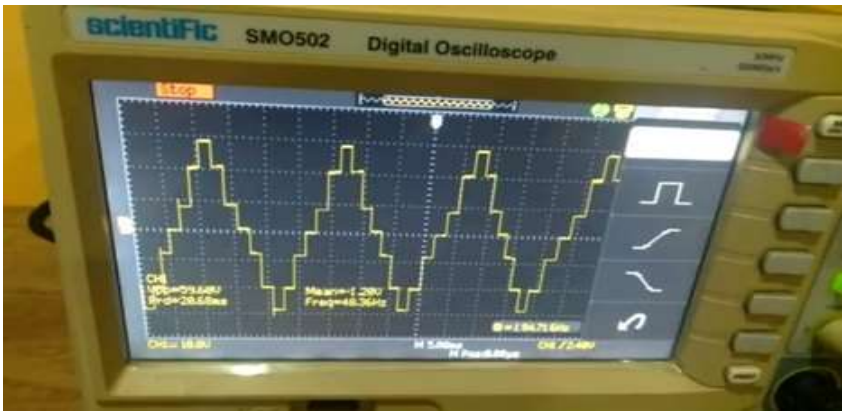

Fig. 12 Measurement of voltage spectrum using DSO

The Table IV is the comparison analysis of the peak-peak line voltage (V_{P-P}) and frequency obtained from MATLAB/Simulink and Hardware setup. The table clearly depicts that the values procured by hardware setup is nearly equal to the simulation results.

Table IV: Performance comparison of seven-level AMLI

Parameter	Simulation result	Experimental result
Peak-peak line voltage(V_{P-P})	60.33 V	59.60 V
Frequency	50 Hz	48.36 Hz

IV. CONCLUSION

In this paper, a seven-level symmetric cascaded multilevel H-bridge (CHB) inverter with lesser switches has been presented. This reduction in switches has not only reduced the cost, complexity, area requirement, and various losses but also improvised the efficiency. The model is based on CHB architecture because of its unique advantages such as the optimum number of levels in the CHB, and the optimum switching frequency so on and so forth. For generation of pulses, level shifted in-phase disposition PWM technique has been selected for the proposed system as it has provided the best performance using soft tools. With satisfactory simulation results from MATLAB/Simulink, this system has been designed and tested in Proteus for hardware implementation. Verified model is then implemented on hardware using MOSFETs and PIC microcontrollers. In order to validate the experimental setup, the voltage spectrum is measured using DSO and it is compared with the result obtained using Simulink model. Consequently, the simulation procured 60.33 V with frequency 50 Hz whereas the hardware setup obtained 59.60 V with frequency 48.36 Hz. It is found that the hardware result agrees with the simulation and thereby it validate the model.

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