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Review and Implementation of 8T SRAM Cell using Tanner tool

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Abstract - The purpose of this study is to build and analyses an 8T SRAM cell employing the Charge Sharing Technique in situations where the performance of a regular 8T SRAM cell decreases with low power supplies. The SRAM cell uses a charge sharing mechanism amongst the transistors in the design to make SRAM more rigid against sounds caused by low power supplies. The read discharge power is utilized in addition to noise reduction. A comparison is given between the regular 6T, 8T, and 8T with charge sharing. It demonstrates that 8T consumes less power with charge sharing than others.

Key Words: 6T SRAM, 8T SRAM.

1.INTRODUCTION

The increased need for portable battery-powered embedded systems necessitated the development of an energy-efficient architecture. As expected, memory will make up 90% of systems, and memory management will become increasingly important. Because of its fast speed, resilience, and ease of manufacture, SRAM is a popular choice for embedded systems. The larger the SRAM cell, the more power it consumes. A basic low-power SRAM cell is created by combining six cross-coupled CMOS inverters into a basic 6T SRAM cell. The power consumption of 6T SRAM becomes substantial with low power sources when technology scales below Nano meters, as the gate delay increases, reducing the frequency of operations. At the cell level of design, an 8T SRAM cell with charge sharing mechanism that was used at the architectural level is implemented.

1.1 SRAM

Several SRAM cell topologies have been reported in recent years. Because of their symmetry in storing logic 'one' and logic 'zero,' resistive load four transistor (4T) SRAM bit cells, load less four transistor (4T) SRAM bit cells, and six transistor(6T) SRAM bit cells have attracted attention in use. The leakage current of the access NMOS transistors ensures information storage within the 4T SRAM cells. As a result, they're not suitable for low-power applications. The information stability of a 6T SRAM cell, on the other hand, is a free lance of the outflow current. Furthermore, the 6T arrangement has a substantially higher noise tolerance, which is a significant benefit, particularly in scaled technologies where noise margins are shrinking. That is the main reason why the 6T SRAM cell is used in low power SRAM units rather than the 4T variants now in use.

Because of its short time period and small size, the Six Transistor SRAM cell is the most commonly used in embedded memory. 6T cell style includes complicated tradeoffs between a variety of parameters, including abrupt area scaling, the most sensible soft error immunity ability, high cell on current, low leakage current through off transistors, and strong stability with minimum voltage and minimum word line voltage pulse. Figure 1 depicts the entire CMOS 6T SRAM bit cell configuration. Full CMOS SRAM configurations offer higher noise margins, lower static or leaky power dissipation, and faster change rates, making them ideal for large density SRAM arrays. Every 6T cell has the capacity to store one byte of data. Two inverters are connected back to back in the 6T SRAM cell.

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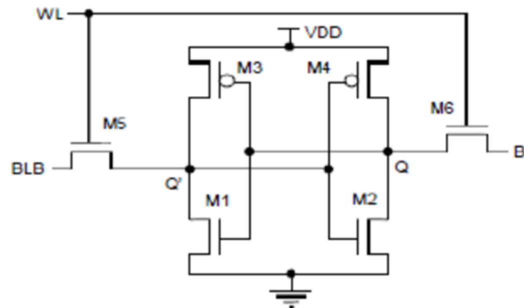

Fig-1: 6T SRAM

The word line (WL) pulse controls the M5 and M6 access transistors. As long as power is available to the 6T bit cell, the cell maintains one of its two potential states, denoted by 0 and 1. In an SRAM memory cell, there are three types of operations: write, browse, and storage. Enabling the word-line enables read and write activities (WL). The value to be written is applied to the bit lines for write operations, and each BL and BLB is recharged to VDD for browse operations. The zero storing node gets upset during the browse operation, which may cause the keep data to be flipped, but the palm write action requires that the information be flipped very quickly. Historically, device size has been chosen to balance the needs of browse and write users.

Two access transistors and two cross coupled CMOS inverters make up the 6T SRAM cell architecture. The input/output ports of a cell with a high capacitive loading are known as bit lines. These bit lines are the sole ones that perform the operations READ and WRITE; we'll look at how they work. It is necessary to write in a certain style. Two cross-coupled CMOS inverters and two NMOS access transistors make up a 6T SRAM cell. The inverters' output (input) creates the internal nodes of cells A and B. Once activated, the access transistors allow the cell's internal nodes to communicate with the cell's input/output ports. Bit lines are the input or output ports of the cell unit of dimension BL. Bit lines unit of dimension a shared data communications medium among the cells on an analogous the same column in an array of cells. As a result, they require a lot of physical phenomenon loading.

Figure 1 depicts how the cell functions during a browse access. Before the cell is accessed, node node a receives a logic 'zero' and node node B receives a logic 'one.' As a result, the transistors M3 and M6 measure 'off,' whilst M4 and M5 live 'on,' catching up on the power supply's escape current and M6. The bit lines are pre charged to VDD before the browse process begins, as is normal. During a read operation on an SRAM cell The read operation begins when the word lines (WL) are enabled, i.e. when the gate of the access transistors is turned on. Because the word lines get more intense, the power supply reaches saturation, whereas M4 runs in the thermionic vacuum tube zone. This linked with power supply has a linear relationship with the voltage of the node 'A' due to the short-channel influence. As a result, during this operation, these transistors behave like a resistance. As a result, provide power and M4 A resistance, and raise node 'A' voltage by V. The input of the convertor M5-M3 is driven by this voltage. to verify the CMOS SRAM: A non-destructive browsing operation V is chosen in such a way that it does not trigger the M5-M3 electrical converter and node B remains at VDD during the cell interval. The constant resistance assumption for M4 during the interval is justified by the continuous voltage of VDD at the gate of M4. the linear model of the bit line discharge path The bit line capacitance of CBL is precharged to VDD throughout this model. CBL cannot discharge and remains at VDD because M1's gate supply voltage remains at zero volts (V_{gs1} = 0V). To supply the regular logic levels, the respectable voltage between BL and BL is amplified employing method electrical equipment.

Clearly, lowering the resistance at intervals along the discharge path results in a faster bit line discharge. However, such improvements come at the cost of bigger cell semiconductor device sizes, which aren't always desirable for high density SRAMs. Traditionally, a DC analysis of the cell transistors' action is used to verify the cell's soundness during the browsing operation. As previously stated, an occasional sufficient V ensures that the output of inverters M5-M3 at node B remains constant. The resistive magnitude relation of power supply and M4 controls the voltage level V to provide a non destructive browsing operation.

The cell's behavior during the write operation. The initial conditions of nodes A and B unit VSS and VDD are shown in this diagram. We have a tendency to focus on improving the knowledge of the cell because re-writing recent data to the cell is trivial. In other words, the write operation is complete when the voltage levels on nodes A and B, respectively, become VDD and VSS. If every bit line unit of measurement is pre charged to VDD, the activation of the word line cannot produce a spare voltage increase on node A to trigger the CMOS inverter M5-M3. As a result, the write operation is carried out by lowering the voltage on the bit line associated with node B, BL (e.g., VSS.) At the start of the process, this procedure creates a possible divider consisting of M5 and power offer.

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2. 8T SRAM

To determine the voltage that emerges at node B when the word lines are activated in a write operation, V. When the voltage is low enough, the convertor M6-M4 is triggered, and node A is charged to VDD. Because node A drives the M5-M3 convertor, node B is forced all the way down to VSS by power offer, and M5 is turned off. As a result, the cell's logic state is altered. When the process is finished, the word line becomes inactive. In most cases, a write operation is bonded by selecting a precise PR. At the input of convertor M6-M4, a lower PR lands up during a lower V, and a lower V is elaborated to higher drive. It's worth noting that the defined type of operation for an associate SRAM cell is frequently configured with the proper selection of the bit line voltage. However, this necessitates the use of extra edge circuits such as bit line pre charge circuits and writing drivers to ensure that the bit line voltage setting is positive and proper before any operation. We tend to employ 8T SRAM cells for rapid transmission applications at low supply voltages due to the soundness constraints of 6T SRAM cells. It's similar to a 6T SRAM cell with an M5 and M6 transistor scan decoupled path. Let's have a look at how an 8T SRAM works.

The write process of an 8T SRAM cell is identical to that of a 6T SRAM cell. The write procedure in 8T SRAM is demonstrated and detailed further down. The bit line must provide zero volts and VDD to the bit line in order to write '0'. (BL bar). The write word line is asserted, causing both transistors M3 and M4 to turn on. As a result, the bit line value is saved at Q. As a result, '0' is saved at Q. Similarly, the letter '1' is most likely carried in the same way. The bit line must have a value of VDD, whereas the bit line bar must have a value of 0 volts. Because WWL is enabled for write operations, the values in bit lines are stored at the applicable nodes, therefore at Q, the value will be logical '1' and at Q bar, it will be logical '0'. When compared to the basic SRAM process, the write operation is unchanged. The read process is started by pre-charging the read bit line to VDD, as in the traditional method. The access transistor M5 is turned on by the read word line (RWL). If the value stored at Q is '0,' transistor M6 will turn on, and RBL will be directly linked to ground via M5&M6 transistor discharges. This means the value stored in the SRAM at Q is zero. Because the M6 transistor is turned off, there is no discharge path for RBL, and the value in RBL is VDD, indicating that the value stored at Q is '1.'

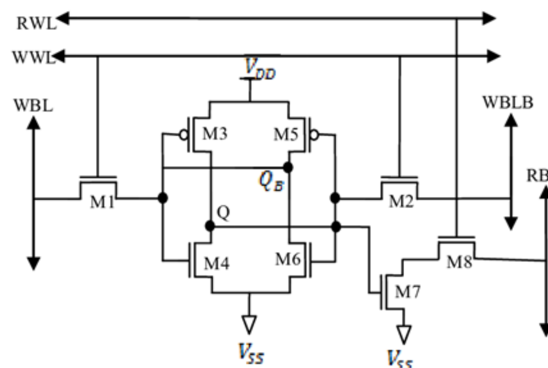

Fig-2: 8T SRAM

Indeed though the transistor count increased the power consumption, the problems of 6T SRAM are minimized in 8T SRAM. It covers the circuit diagram and operations of conventional and 8T SRAM. The next topic is the SRAM with charge sharing concept. The suggested SRAM design employs the charge sharing principle of a 10T SRAM system. However, as comparison to the previous 10T SRAM, the proposed design uses smaller transistors, which reduces the system's space and power consumption. A single concluded 7T bit cell with one bit line (BL) for write operation and one Read Bit cell for read operation makes up the proposed SRAM. WWL was enabled throughout the write process, but RWL was impaired (i.e. RWL='0'), hence M4, M5, M6 are in the off state. The cell functions as a single ended 5T SRAM cell, writing Bit line data to the P1 M3 and P2 M2 cross-coupled inverter pairs. Because WWL='0' during the read phase, the bit line separated from the inverter pair, and RWL was enabled, M6 M5 will be in the ON state. Rather of using the same BL for read operations, we use a separate bit line called RBL. As a result, RBL was pre charged during the read operation. M4 was in the OFF state when reading '1', hence there was no discharging path for RBL to discharge, so the charge was maintained and the '1' was read.

3.RESULT

Tanner Tools 13.0's S-edit and T-Spice are used to design and simulate these SRAM designs, which use TSMC018 technology. The power dissipations of the conventional 8T SRAM and the proposed SRAM are compared and displayed.

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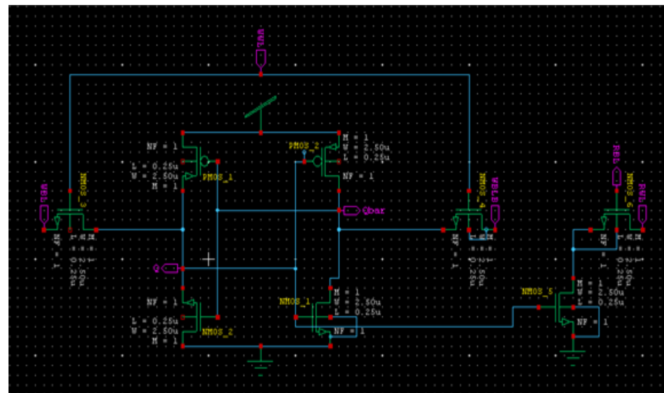

Fig3: 8T SRAM Schematic

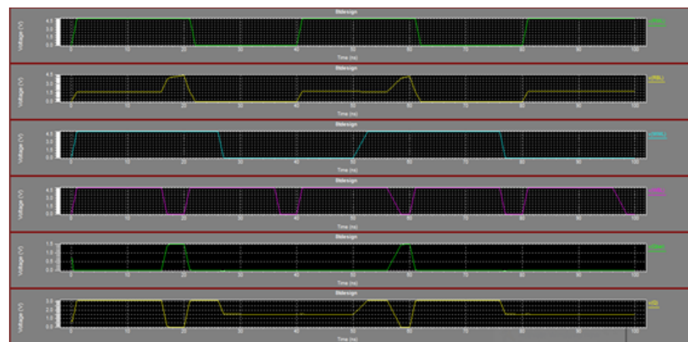

Fig -4: 8T SRAM Waveform

4. CONCLUSIONS

S:no	Types of SRAM	Write		Read	
		Current (max)	Power (max)	Current (max)	Power (max)
1	6T	400µA	60µw	500nA	100µW
2	8T	400µA	negligible	400nA	60µW

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