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Home Automation based on FPGA through a Wireless Server

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Abstract: This project describes the techniques for designing, implementing, and controlling a home automation system using FPGA through a wireless server. Home automation systems have fascinated considerable attention with the advancement of Future Home. Smart Home is an automated home system in that each device has sensors, actuators, and controllers connected through Wi-Fi so we can control them whether you're at home or miles away. It enhances comfort, automation, and safety. It also gives security for a better life quality for residents. We all know that many automation systems have evolved in recent years. Mostly home automation systems are built for short ranges using Bluetooth, Wi-Fi, and GSM modules. The most important part of this project is to develop home automation using FPGA through a wireless server so that we can control the home appliances remotely. FPGA - Field Programmable Gate Array used for expanding the home automation in the future. By using the FPGA we can collect the data and control or access the digital-led switches. Mainly the proposed system aims to cover end-to-end Smart Home appliances using FPGA instead of microcontrollers. However, FPGA that acts as a processor and a controller is used to collect data and process it more efficiently in place of a microcontroller. The advantage of using FPGA is that we can extend it to various appliances for future needs.

Keywords: FPGA, IoT, Zedboard, ESP8266

INTRODUCTION

The Internet of things makes the home Smarter that allows users to control and monitor home appliances using the Internet. IoT is a design of interrelated computing devices that can communicate data through a server without requiring human interaction. The smart home is an umbrella term for the automation, digitization, and interconnecting of home automation. All home automation system refers to IoT devices that can be automated using real-time over the Internet. Home automation works through devices that are connected to the Internet. Nowadays, homes have some “smartness technology” because various devices have built-in sensors and controllers which adapt to environmental conditions. Smart Home devices can be linked through a Wi-Fi router is an access point (AP) to control home appliances. These connected devices can be managed or controlled in several ways like Voice Assistant, web page, or an app. Home automation works on three criteria monitoring, control, and automation. A Smart home enhances the security and safety of the house, which can detect people and control the doors without interaction. There are a lot of benefits to using IoT devices like productivity improvement, predictive analysis, rapid response, reduction of human errors, security improvements, cost efficiency, and collaboration with AI technology. Thus smart home makes our life easier, safer, and more convenient. Fig 1 shows the home automation setup.

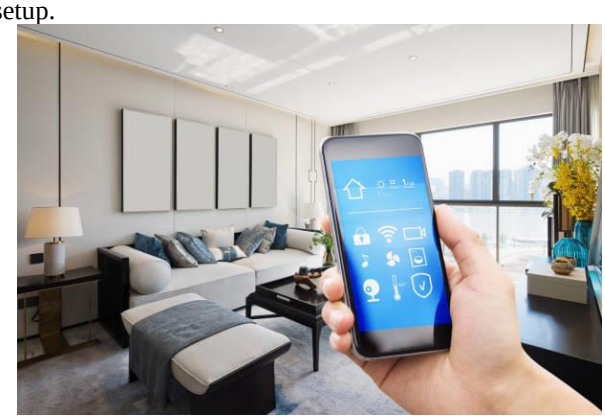

Fig 1: Home Automation Setup

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METHODOLOGY

In designing a home automation system, one or more suitable platforms are used for building a reliable and flexible system that can be easily operated and adapted for a new household appliance. Therefore, for this project, some specific choices were made on the type of platform, hardware components, and mode of operation of the home automation system. We designed the system based on FPGA, Wi-Fi, and relay modules. FPGA can be controlled and automated by various devices by using one board. The system consists of two primary components FPGA and the Wi-Fi module. The Wi-Fi connects the FPGA with the J-channel. By connecting with Wi-Fi, we can automate the appliances at home. The Wi-Fi router acts as the access point (AP) and is identified by its SSID (Service Set Identifier). By Interfacing the FPGA and Wi-Fi module, we can connect to the Wi-Fi server using the IP address. After connecting with the Wi-Fi, we can control the led switches. By interfacing the relay module to the led, we can operate the relay to turn on and off.

HARDWARE REQUIREMENT

FPGA(Zedboard): Zedboard was developed for the wireless control of home appliances, such as lights, sensors, door locks, thermostats, and similar. Through the use of Zedboard, a house or home becomes smart. The main objective of a smart home is to make your life simpler, easier, and, more pleasant and to increase your security and comfort. And this is where Z-board comes in. The ZedBoard is a low-cost development board for the Zynq-7000 all programmable SoC (APSoC). Zynq-7000 APSoCs have a tightly coupled ARM processing system and 7-Series programmable logic to create unique and powerful designs. It has three types of memory. They are 512Mb of DDR3 RAM, 256Mb of Quad-SPI FLASH memory, and 4GB of SD card. It has a USB-JTAG programming port, USB OTG, and a USB-UART port. It has a processing system and programmable logic Input/Output expansion (FMC, Pmod, XADC) for easy user access. It contains I²S audio CODEC. It meets all the requisites for creating the ideal smart home and smart living: reliable and secure communication, simple installation, low power consumption, remote or local control, several available devices, interoperability, and affordability

Wi-Fi Module: ESP8266 is a Wi-Fi-enabled system-on-chip (SoC) module developed by the Espressif system. It is used for the development of IoT applications. It can provide internet connectivity to all IoT applications. It has the capability to be used as Station as well as Access Point or both combined. It supports serial communication and is compatible with many development platforms like Arduino. It employs a 32-bit RISC CPU at 80 MHz. It comprises 64 KB boot ROM with 64 KB instruction RAM and 96 KB data RAM. It utilizes flash memory and can facilitate all IoT developments.

Relay Module: In a 5V 4-channel relay interface board, each channel needs a 15-20mA driver current. The board has Some input pins like Vcc is a system power source, jD_VCC is the relay power source, GND is the Ground pin, and IN1-IN4 relay control port and the maximum output of the relay is DC 30V/10A, AC 250V/10A. The relay terminal (COM, NO, and NC) comes with a LED to indicate the status of the relay.

PROPOSED SYSTEM

A practical approach to design, fabrication, and validation of an IoT-based portable automation system called IoT Home for Smart Homes. The main contribution of the system is to automate home appliances like doors and electrical appliances from anywhere using the cloud server. It enables IoT automation and automation of Smart Home by using FPGA and a Cloud-based Server. Bluetooth technology is useful when transferring information between two or more devices near each other when data transmitting speed is not an issue, such as telephones, printers, modems, and headsets. It is best suited to low-bandwidth applications like transferring sound data with telephones or byte data with hand-held computers (transferring files) or keyboards. Wi-Fi is better suited for operating full-scale networks because it enables a faster connection, better range from the base station, and better wireless than Bluetooth Mainly, the proposed system aims to cover end-to-end smart home automation that can be accessed from anywhere globally, and also the advantage is FPGA process instruction in parallel processing. It increases safety and security and enhances life quality and convenience. The block diagram of the proposed system is shown in fig 2. The circuit diagram of the proposed system is shown in fig 3.

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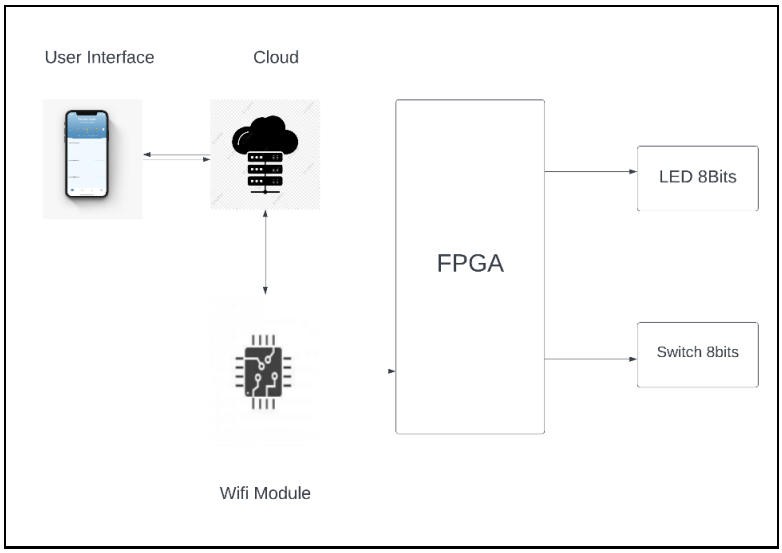

Fig.2: Block Diagram of Proposed System

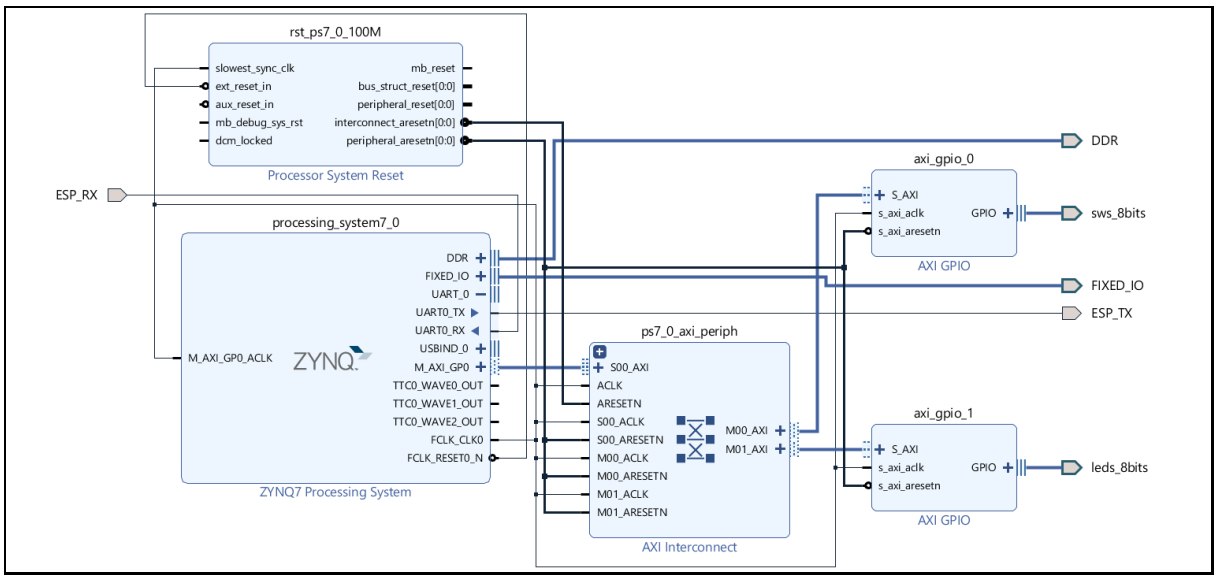

Fig.3: Circuit Diagram of Proposed system

WORKING

Software Implementation:

This software implementation constructs the circuit to interface the Wi-Fi module and Zedboard. Connection of DDR pins into ZYNQ 7000 Processor and connection for fixed I/O pins into LEDs 8bits and switch 8bits outputs. Simulating the circuit to generate an approximate gain for system running time for the calculated gain.

The value is

- run: Time (s): CPU = 00:00:06 ; elapsed = 00:01:58, Memory (MB): peak = 2862.719 ; gain = 0.000.
- x-sim: Time(s): CPU = 00:00:18; elapsed=00:02:17, Memory (MB): peak = 2862.719; gain = 8.645.
- launch simulation: Time (s): CPU = 00:00:34; elapsed = 00:04:21. Memory (MB): peak = 2862.719; gain = 27.012

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- Clock pulse of FPGA is edges are rise -rise, worst negation slack = 3.773 ns, total negative slack =0, total endpoints = 1814 ns.

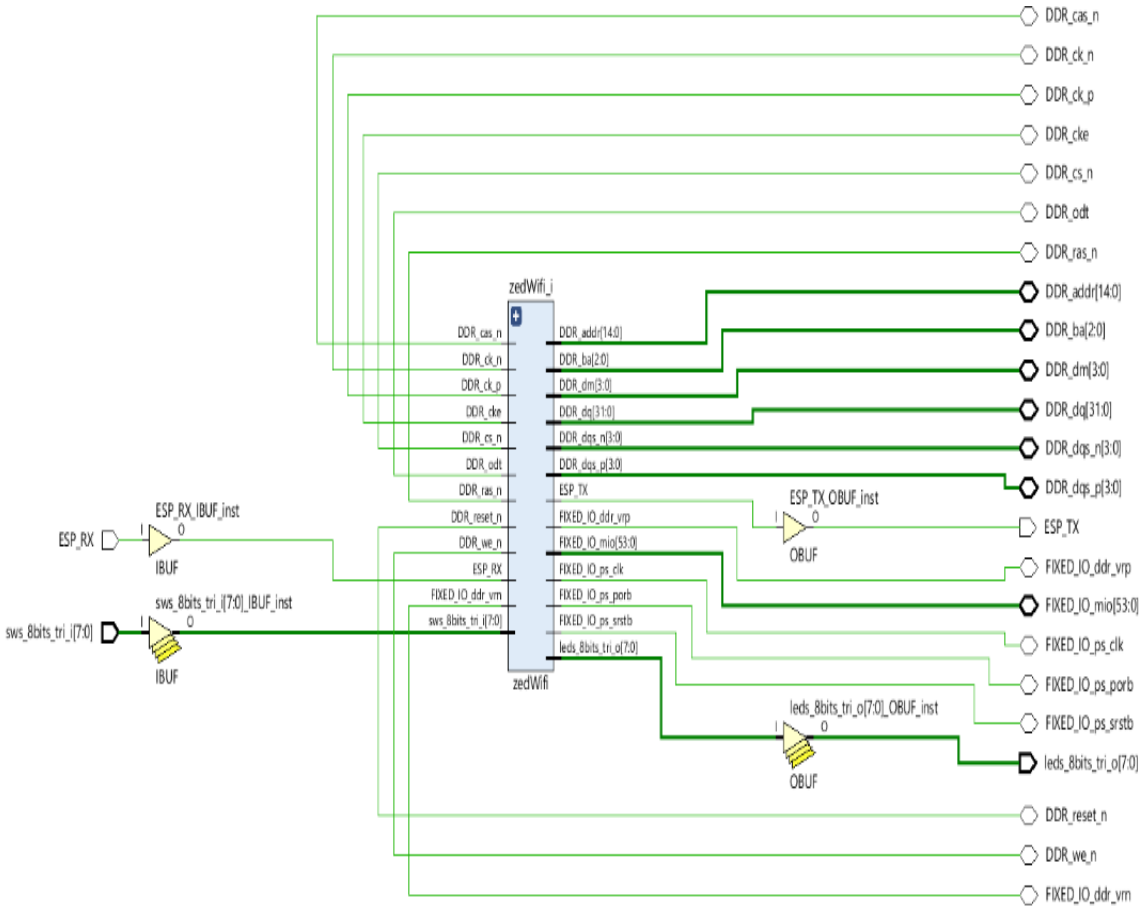

Fig 4. Simulation Circuit Diagram

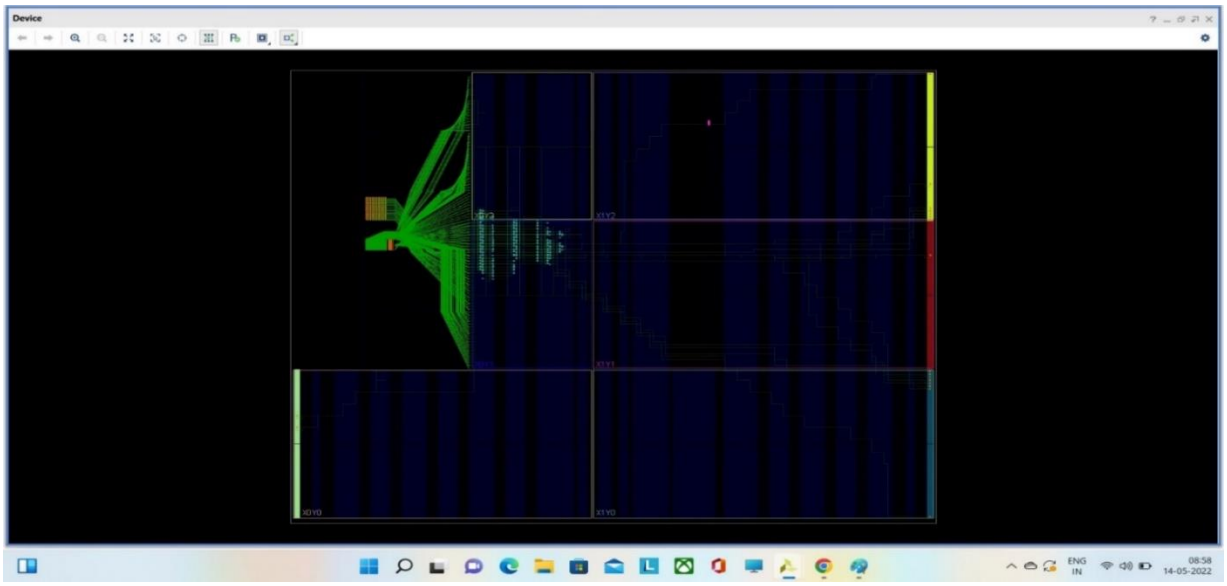

Fig 5. Device Interior Connection

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TOTAL POWER OF THE CIRCUIT CONSUMING:

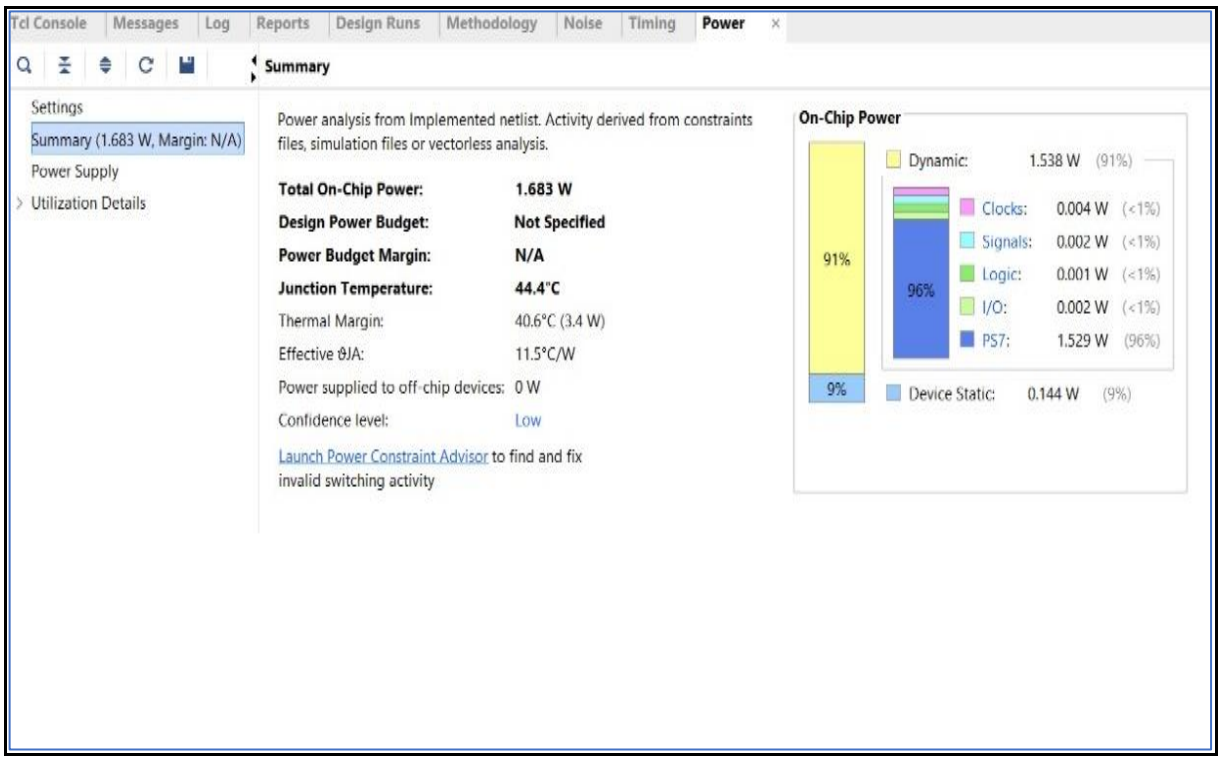
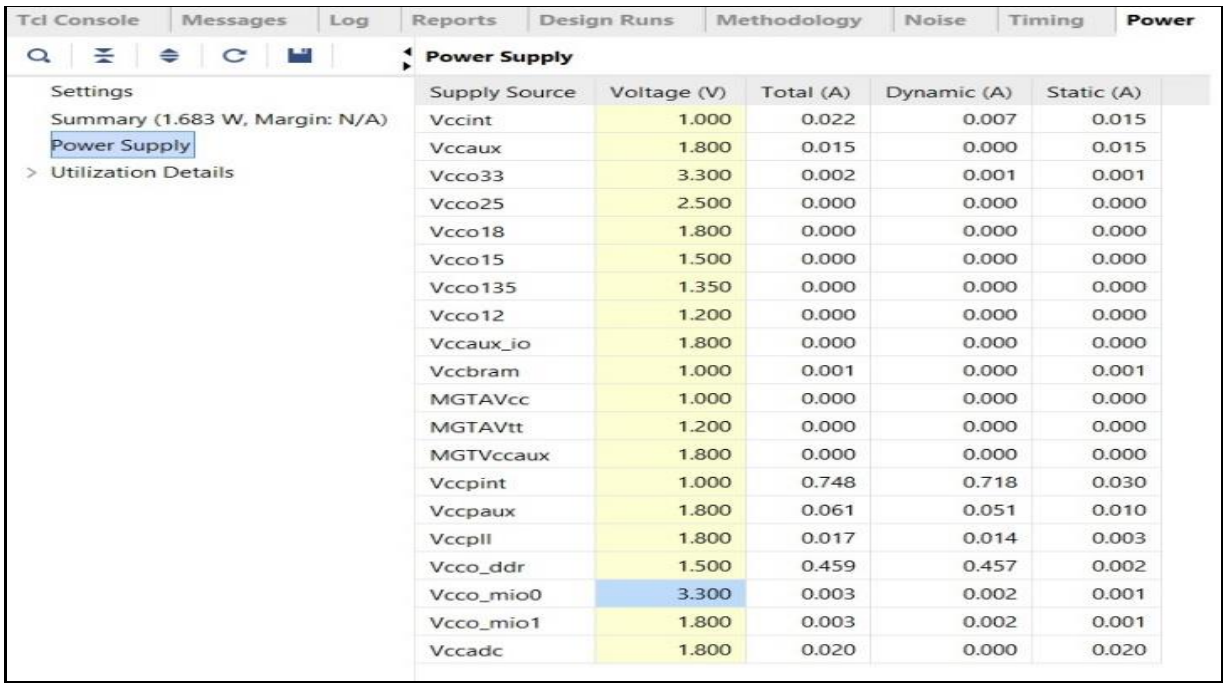


Fig 6. Total Power Summary



Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	0.022	0.007	0.015
Vccaux	1.800	0.015	0.000	0.015
Vcco33	3.300	0.002	0.001	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.001	0.000	0.001
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
MGTVccaux	1.800	0.000	0.000	0.000
Vccpint	1.000	0.748	0.718	0.030
Vccpaux	1.800	0.061	0.051	0.010
Vccpll	1.800	0.017	0.014	0.003
Vcco_ddr	1.500	0.459	0.457	0.002
Vcco_mio0	3.300	0.003	0.002	0.001
Vcco_mio1	1.800	0.003	0.002	0.001
Vccadc	1.800	0.020	0.000	0.020

Fig 7. Table Of Power Supply For All Pins

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Tcl Console | Messages | Log | Reports | Design Runs | Methodology | Noise | Timing | Power

Summary
Messages (2)
I/O Bank Details
Links

I/O Bank Details

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin...	Notes
I/O Bank 0 (0)								
I/O Bank 13 (1)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
AA11	ESP_TX	LVCMOS33	3.30	SLOW	12	FP_VTT_50	99.40	
I/O Bank 33 (8)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
T22	leds_8bits_tri_o[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	51.27	
T21	leds_8bits_tri_o[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	77.68	
U22	leds_8bits_tri_o[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	46.76	
U21	leds_8bits_tri_o[3]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	79.84	
V22	leds_8bits_tri_o[4]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	64.82	
W22	leds_8bits_tri_o[5]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	59.27	
U19	leds_8bits_tri_o[6]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	95.97	
U14	leds_8bits_tri_o[7]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	98.22	
I/O Bank 34 (0)								
I/O Bank 35 (0)								

Fig 8.Table Of Noise Rate For I/O Bank Details

HARDWARE IMPLEMENTATION

The project contains the setup of FPGA (Zedboard ZYNQ) and Wi-Fi module ESP8266. By interfacing the Wi-Fi module to the Zedboard using its J-channel that has GPIO pin, Transmitter, and receiver pins. Implementing the C++ program for connecting the Wi-Fi module to the Wi-Fi router. After Starting the HTTP server, we can use the IP address of the Wi-Fi router to send data from the device and execute it in the led 8bits. The proposed system model is pictured in Fig. 7 The 8bit LEDs are turned on according to the input data which has been given by the user. The Input data and output of the led 8 bits in the proposed system are pictured in Fig. 8 and Fig. 9. We can also collect the data on LED's switch position from Zedboard. The Switch position of the board and output of the switch position are pictured in Fig. 10 and Fig. 11.

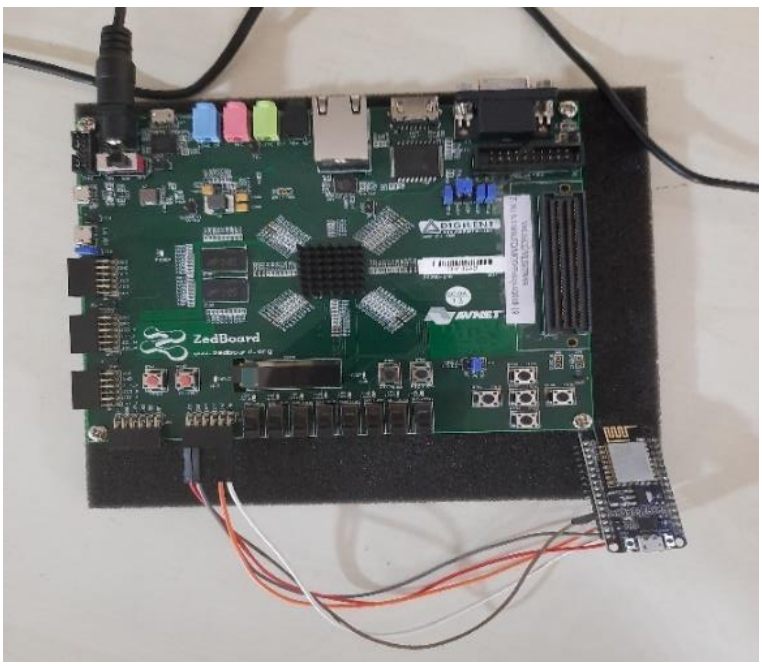

Fig 9. Model of proposed System

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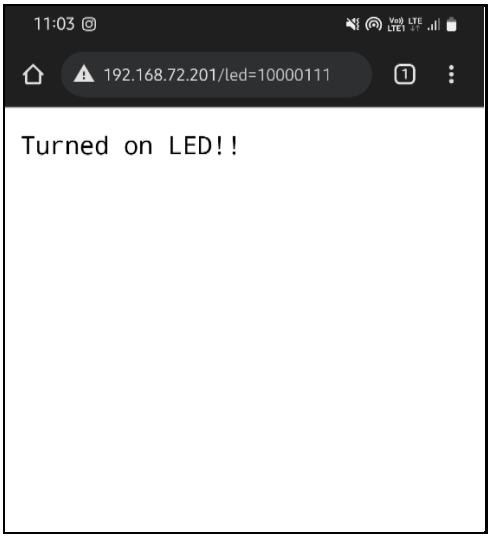

Fig 10. Input data of LEDs

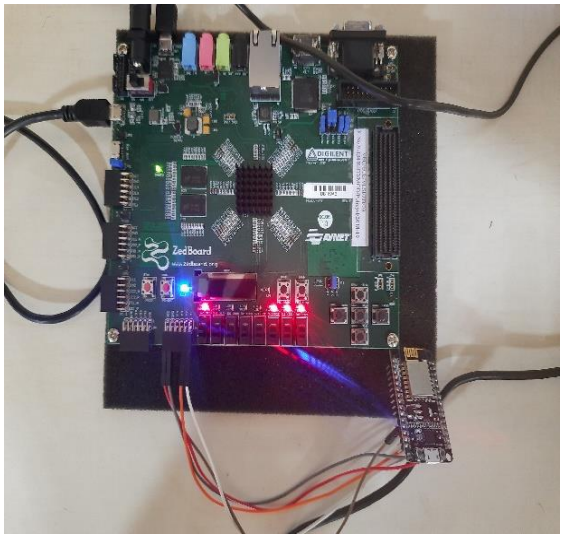

Fig 11. The output of led 8bits

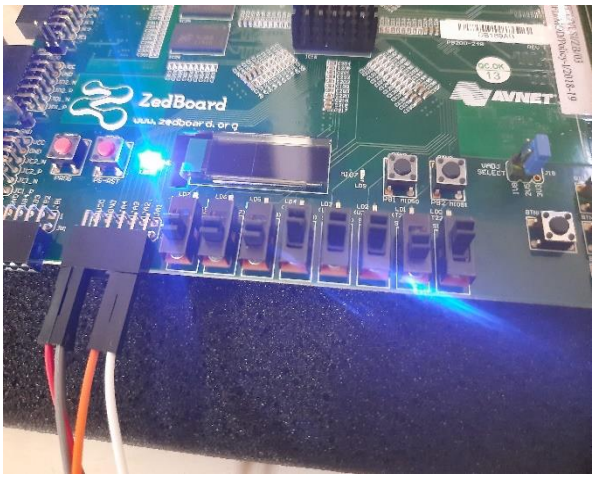

Fig 12. Switch Positions on Board

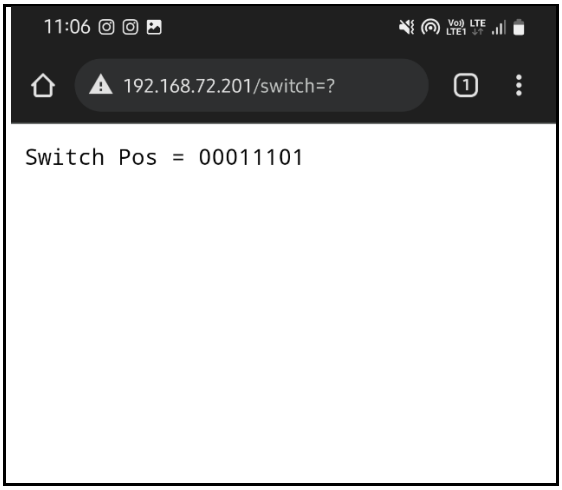

Fig 13. The output of Switch Position

CONCLUSION

This Project has the potential to create a revolution in home automation systems. The FPGA had selected as, compared to microcontrollers, it provides many input/output ports and the parallel implementation of hardware results in faster algorithm execution. The user interface on the mobile phone communicates with the FPGA using the Wi-Fi interface. Our future work will concentrate on including various devices to expand home appliances. So that the proposed system of real-time automation can be made universal.

REFERENCES

[1] G. Prakash, K. Sathishkumar, B. Sakthibharathi, S. Saravanan and R. Vijaysai, "Achieveing reduced area by Multi-bit Flip flop design," 2013 International Conference on Computer Communication and Informatics, 2013, pp. 1-4, doi: 10.1109/ICCCI.2013.6466259.

[2] Dongyoun Yi and T. Kim, "Allocation of multi-bit flip-flops in logic synthesis for power optimization," 2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016, pp. 1-6, doi: 10.1145/2966986.2966998.

[3] C. Münch, R. Bishnoi and M. B. Tahoori, "Multi-bit non-volatile spintronic flip-flop," 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2018, pp. 1229-1234, doi: 10.23919/DATE.2018.8342203.

DOI: 10.17148/IJIREEICE.2022.10505

[4] P. Arunraj and S. Hiremath, "Design of Sequential Circuit Using Data Driven Clock Gating and Multibit Flip-Flop Integration," 2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA), 2019, pp. 1195-1199, doi: 10.1109/ICECA.2019.8821940.

[5] J. -F. Lin, M. -H. Sheu, Y. -T. Hwang, C. -S. Wong and M. -Y. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 3033-3044, Nov. 2017, doi: 10.1109/TVLSI.2017.2729884.

[6] Chen-Hsien Lin, Shih-Hsu Huang, Jia-Hong Jian and Xin-Jia Chen, "New activity-driven clock tree design methodology for low power clock gating," 2017 6th International Symposium on Next Generation Electronics (ISNE), 2017, pp. 1-3, doi: 10.1109/ISNE.2017.7968741.

[7] H. Moon and T. Kim, "Design and allocation of loosely coupled multi-bit flip-flops for power reduction in post-placement optimization," 2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC), 2016, pp. 268-273, doi: 10.1109/ASPDAC.2016.7428022.

[8] R. Arun Prasath, I. Divona Priscilla and P. Ganesh Kumar, "A high speed proficient power reduction method using clustering based flip flop merging," 2014 International Conference on Communication and Signal Processing, 2014, pp. 1424-1429, doi: 10.1109/ICCSP.2014.6950084.

[9] L. Cherif, M. Chentouf, J. Benallal, M. Darmi, R. Elgouri and N. Hmina, "Usage and impact of multi-bit flip-flops low power methodology on physical implementation," 2018 4th International Conference on Optimization and Applications (ICOA), 2018, pp. 1-5, doi: 10.1109/ICOA.2018.8370498.

[10] N. B. Rizvandi, S. A. M. Barandagh and A. Khademzadeh, "Power dissipation and gate number reduction of a utilized register, replaced by equivalent counters," 2004 24th International Conference on Microelectronics (IEEE Cat. No.04TH8716), 2004, pp. 789-791 vol.2, doi: 10.1109/ICMEL.2004.1314952.