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Low Power Based Dynamic True Single Phase Clock [Tspc] D Flip Flop For High Performance Application

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Abstract: D flip-flop is viewed as the most basic memory cell in by far most of computerized circuits, which brings it broad usage, particularly under current conditions where high-thickness pipeline innovation is as often as possible, utilized in advanced coordinated circuits. As a constant research center, various types of zero flip-flops have been explored, and the ongoing exploration pattern has gone to rapid low-control execution, which can come down to low power-defer item.To actualize superior VLSI, picking the most proper D flip-flop has clearly become an incredibly huge part in the structure stream.This work includes to design and development of a Low Power Dynamic Power Based True Single Phase D Flip Flop [TSPC] for High Performance Application using Cadence Tool. The design has been tested and verified using Cadence Virtuoso. The developed TSPC D Flip Flop model can be used in the design of sequential circuits with enhanced performance.

Keywords: TSPC D Flip-Flop, Low Power VLSI, Design, High-Speed Sequential, Circuits, Cadence Virtuoso Simulation

I. INTRODUCTION

In modern digital systems—especially those aimed at high-performance and portable applications—power efficiency and speed are critical design parameters. Flip-flops, as fundamental building blocks of synchronous systems, markedly influence both power consumption and timing performance. Among various architectures, the True Single Phase Clock (TSPC) approach is particularly compelling due to its use of a single-phase clock, enabling high speed and low clock loading while simplifying clock distribution [1], [2].

The Dynamic TSPC D flip-flop leverages dynamic logic and a minimized transistor count to reduce propagation delay and dynamic power dissipation. It avoids complex multi-phase or complementary clock networks and mitigates clock skew—making it ideal for deep pipeline and high-frequency applications such as microprocessors and DSPs [3], [4]. By optimizing transistor sizing and internal node structure, TSPC designs can deliver significantly lower power-delay product (PDP) compared to conventional TG-based designs [5].

With ongoing CMOS scaling and pervasive demand for high-speed, energy-efficient architectures, sequential elements such as flip-flops have become critical optimization targets. Research—including that by Lin et al. (2017) on a 19-transistor low-power TSPC D-FF—demonstrates up to 63% PDP improvement and considerable area savings in 90 nm technology [5]. More recently, retentive and redundant-precharge-free TSPC variants have been introduced, offering enhanced robustness, lower leakage, and better energy efficiency in sub-threshold and near-threshold regimes [6].

TSPC flip-flops typically use precharge and evaluate phases driven by the same clock edge, passing data through transmission gates or pass transistors and storing it in dynamic nodes. This achieves fast clock-to-Q response, minimal clock loading, and reduced transition count, aligning with power-aware design philosophies [3], [5].

However, the dynamic nature of TSPC circuits introduces challenges such as charge sharing, leakage, and noise sensitivity. To address these, advanced designs incorporate techniques like transistor sizing optimization, keeper circuits, data-dependent precharge schemes, and MTCMOS approaches to suppress leakage without sacrificing speed [4], [6]. These enhancements ensure that TSPC flip-flops remain viable and advantageous in modern, ultra-scaled VLSI systems.

The main objective of our work is to design a low power, high speed True single Phase Clock [TSPC] D Flip Flop with optimized transistor sizing and clocking for minimal power, low delay, and efficient switching

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II. METHODOLOGY

The methodology adopted for designing and Comparison an TSPC D FLIP FLOP With D flip flop using CMOS technology involves a systematic design flow, simulation, and validation process. The entire process is divided into six key blocks as outlined below in Fig. 1 each representing a crucial phase in the development and optimization of the system.

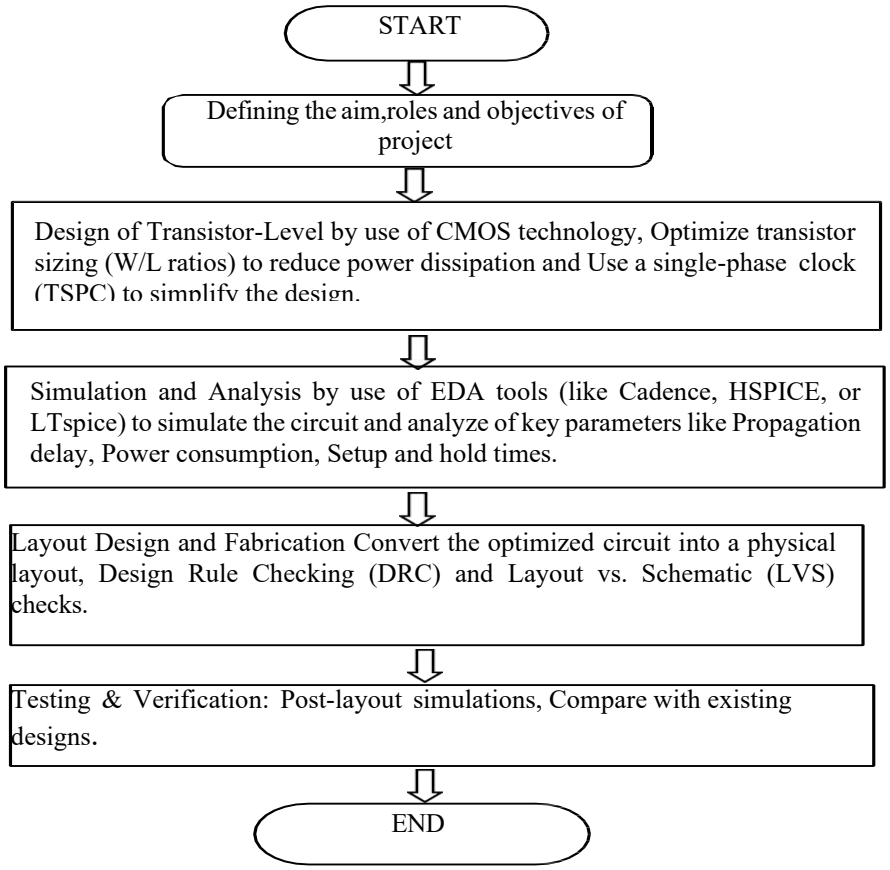

Fig. 1 FLOW CHART: Methodology Flow for TSPC D Flip Flop Design using CMOS Technology

Schematic Design of Conventional D Flip-Flop: The conventional (static) D flip-flop is designed using basic CMOS logic. It ensures data transfer on a specific clock edge (usually rising or falling). This type of flip-flop is typically composed of logic gates such as NAND, NOR, inverters, and transmission gates, depending on the implementation style (e.g., master–slave or transmission-gate based). The objective of this design is to construct a reliable and functional circuit that captures the input (D) on the clock edge and holds it at the output (Q) until the next clock event.

Key features:

- Edge-triggered behavior (positive or negative clock edge)
- Simple clocking but requires multiple phases if cascaded
- Robust against noise due to full static CMOS logic
- Higher power and area compared to dynamic logic

Schematic Design of TSPC D Flip-Flop: The True Single Phase Clock (TSPC) D flip-flop is based on dynamic logic principles and introduced to improve speed and reduce power consumption by eliminating the need for multiple clock phases. TSPC flip-flops operate with a single-phase clock and combine dynamic and static stages for storage and transition.

Design characteristics:

- Faster operation due to fewer clocked transistors

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- Reduced power consumption since it avoids clock overlap and race conditions
- Suitable for high-speed, low-power VLSI applications
- Relies on charge storage, which makes it more susceptible to noise and leakage when idle

This design involves selecting the appropriate topology (e.g., three-stage TSPC D flip-flop), setting transistor sizing, and validating functionality through simulation.

Transient Analysis / Simulation: After schematic design, both flip-flops are subjected to transient simulations. This time-based analysis applies input signals (D and CLK) while monitoring the output (Q).
Performance metrics include:

- Propagation delay (tpd)
- Setup time (tsu)
- Hold time (th)
- Average dynamic and static power consumption
- Rise/fall times of the output

Simulations are carried out using Cadence Virtuoso.

Layout Design: Following schematic verification, the layout of both flip-flops is implemented using physical design tools. The layout involves defining mask layers such as diffusion, poly, and metal interconnects for fabrication.
Key considerations:

- Area minimization for higher density and lower cost
- Matching and symmetry for reduced skew and balanced switching
- Proper clock routing to minimize delay and skew
- Noise isolation, particularly important in TSPC designs

Once the layouts are complete:

- Design Rule Check (DRC) ensures compliance with fabrication rules such as spacing, minimum widths, and enclosure requirements.
- Layout Versus Schematic (LVS) confirms that the extracted layout netlist matches the schematic netlist.

Both steps are mandatory before fabrication or advanced simulations.

Post-layout analysis includes parasitic extraction, where resistance and capacitance from interconnects are added to the design netlist. This step ensures realistic evaluation of:

- Delay degradation caused by parasitics
- Power variations due to interconnect resistance
- Signal integrity and performance under actual silicon conditions

III. DESIGN AND IMPLEMENTATION

The work is implemented using **Cadence Virtuoso** with 45nm CMOS models. The TSPC-based D flip-flop eliminates complex master–slave structures by using dynamic logic and single-phase clocking. The goal is to design a compact, robust, and energy-efficient sequential element for high-performance VLSI systems such as registers, counters, and shift registers.

CMOS-Based Implementation of D Flip-Flop

The conventional D flip-flop stores one bit of data and can be designed using NAND or NOR gates. It introduces delay in timing circuits, acts as a buffer, and serves as a building block for shift registers.

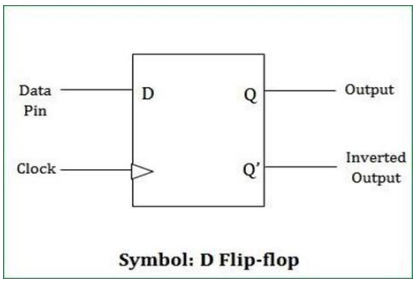

Fig.2**:** Symbol of a D Flip-Flop

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Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Fig.3: Truth table of a D flip flop

On the active edge of the clock, the input data (D) is transferred to the output (Q).

Design Methodology

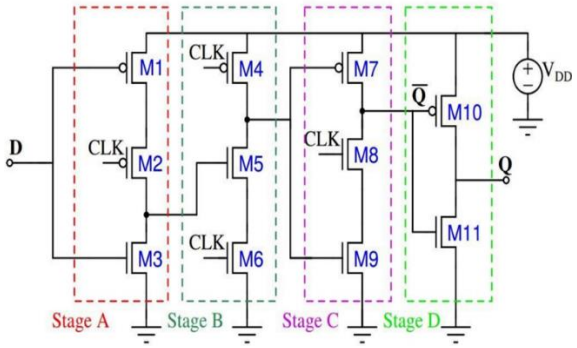

Fig. 4: Equivalent Transistor Sizing Calculation

The TSPC flip-flop design involves equivalent transistor sizing, schematic creation, and simulation.
Transistor sizing ensures balanced rise/fall times, robust logic levels, and optimized performance in 45nm CMOS.

TSPC D Flip-Flop Architecture

The TSPC D Flip-Flop uses three main stages:

1. Dynamic inverter for data sampling.
2. Clock-controlled inverter for evaluation.
3. Static inverter for storage and output.

Key advantages:

- Single-phase clocking → reduces skew and simplifies distribution.
- Low setup/hold time → flexible timing.
- Reduced transistor count (11 transistors).
- Full swing operation → improved reliability.

Schematic Diagram:

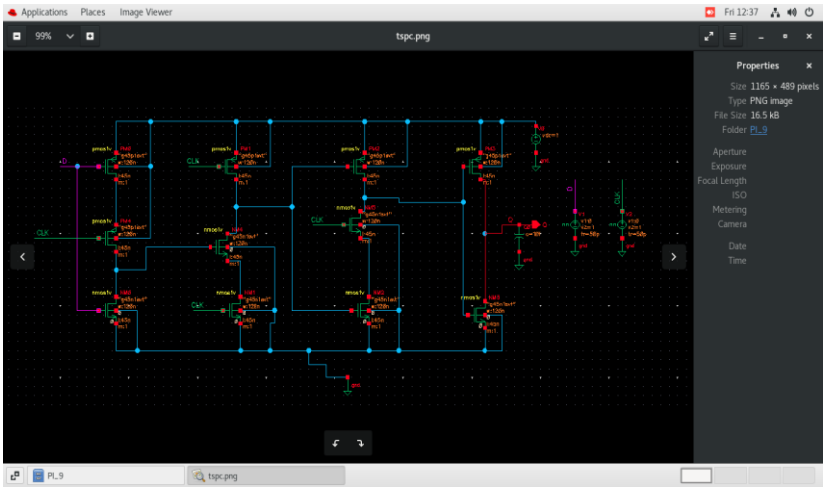

Fig. 5: Schematic of TSPC D Flip-Flop

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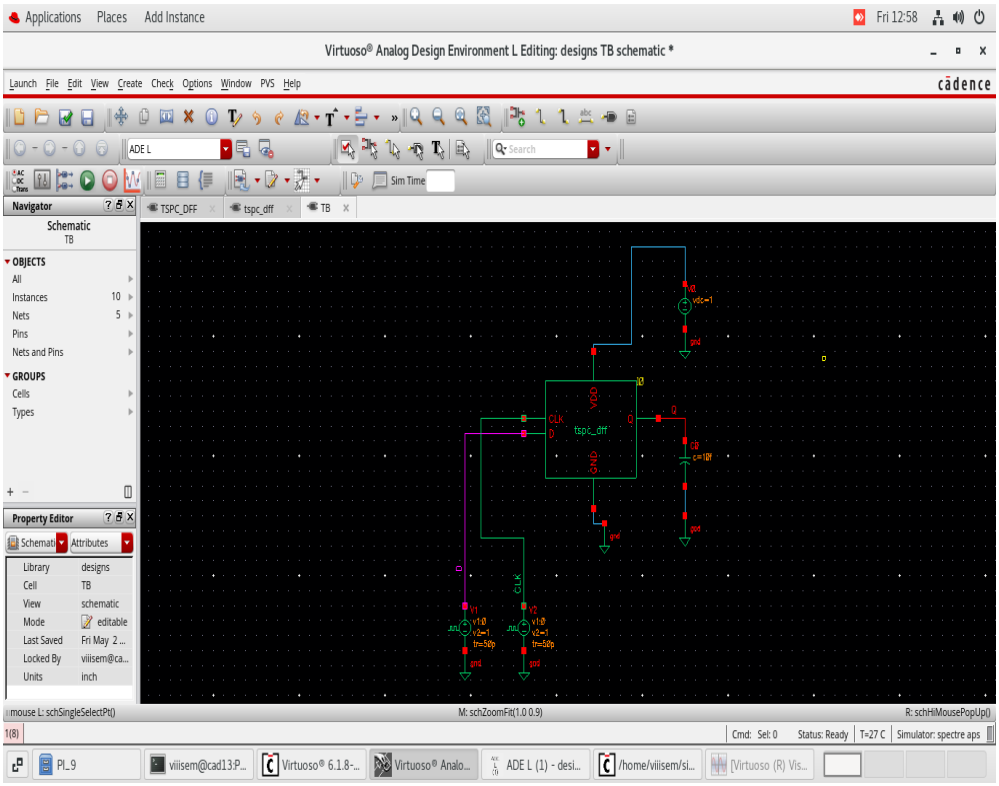

Fig.6: Symbol of TSPC D Flip Flop

The Figure 5 and 6 are Schemetic and Symbol of TSPC D Flip Flop designed in Cadence Virtuoso with PMOS (pmos4v) and NMOS (nmos4v) devices. Clock-driven transistors control intermediate nodes to ensure correct data transfer from D to Q.

SISO Shift Register:

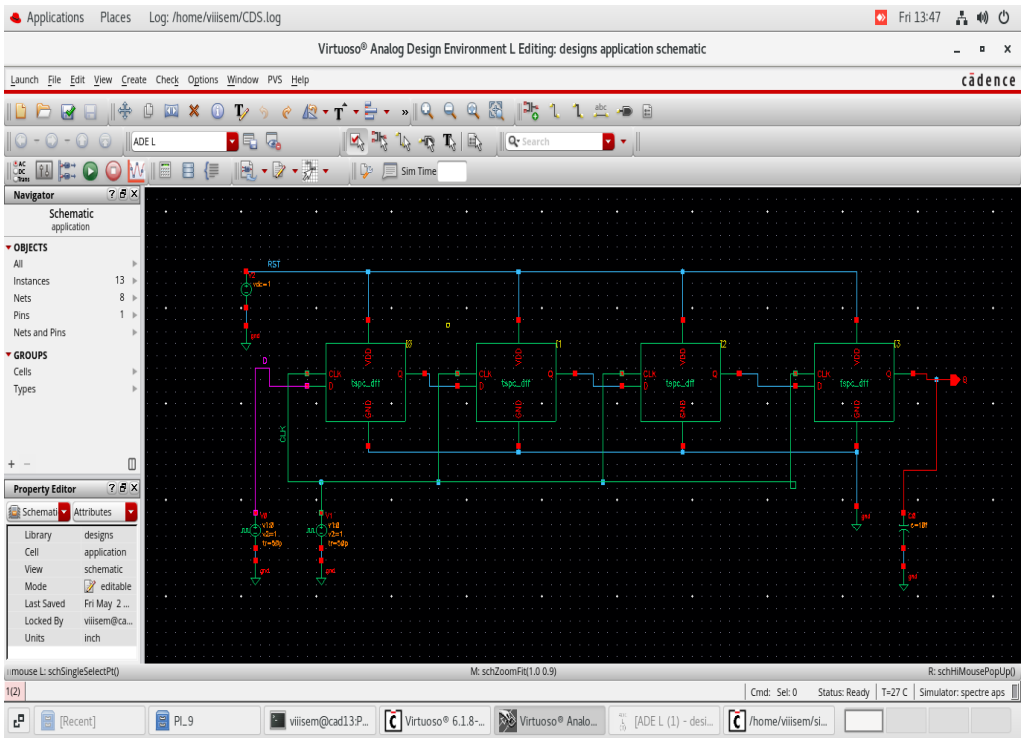

Fig 7: Schematic Of SISO Shift Register

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As an application we implemented SISO Shift Register from the designed TSPC D Flip-Flop. The shift register stores and shifts binary data serially with each clock pulse, using a chain of TSPC flip-flops. TSPC design ensures high-speed operation and low power consumption, making it suitable for high-performance VLSI systems where clock simplicity and energy efficiency are crucial. The design ensures low power and high speed, suitable for modern VLSI systems.

IV. RESULT AND DISCUSSION

Testbench Setup
Simulation is performed in Cadence Virtuoso ADE L.

- Clock period: 1 ns
- Supply voltage: 1.2 V
- Transient analysis duration: 20 ns

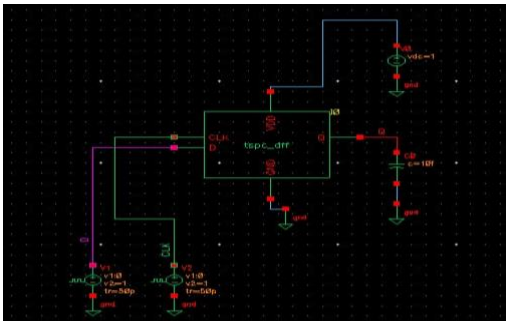

Fig.8: Testbench Circuit

Fig. 9: ADEL Setup Window for SISO Shift Register

Transient Analysis:
The waveform in Fig. 10 demonstrates correct data propagation across all flip-flops. Each bit from Din appears sequentially at Dout after a fixed delay of one clock cycle per stage. The timing diagram confirms glitch-free operation and the correct timing behavior of the register.

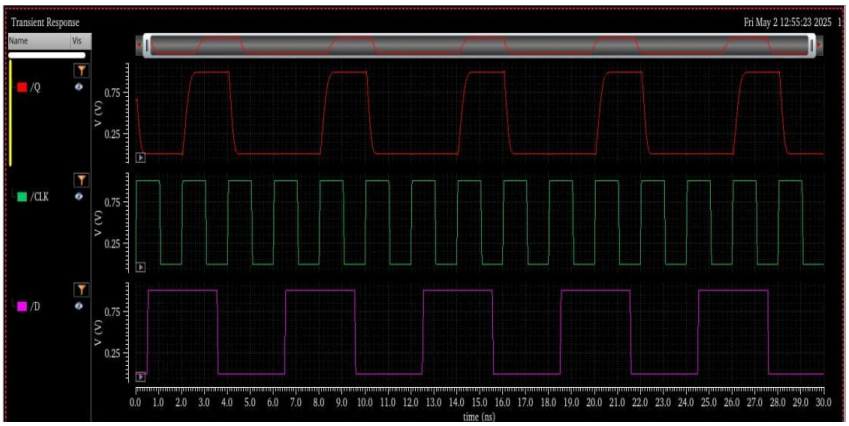

Fig. 10: Transient Simulation of TSPC D Flip-Flop

Transient Simulation of SISO Shift Register:
This Fig. 11 shows serial data shifting through each flip-flop stage with every clock pulse. Output confirms correct sequential propagation from input to output across clock cycles.

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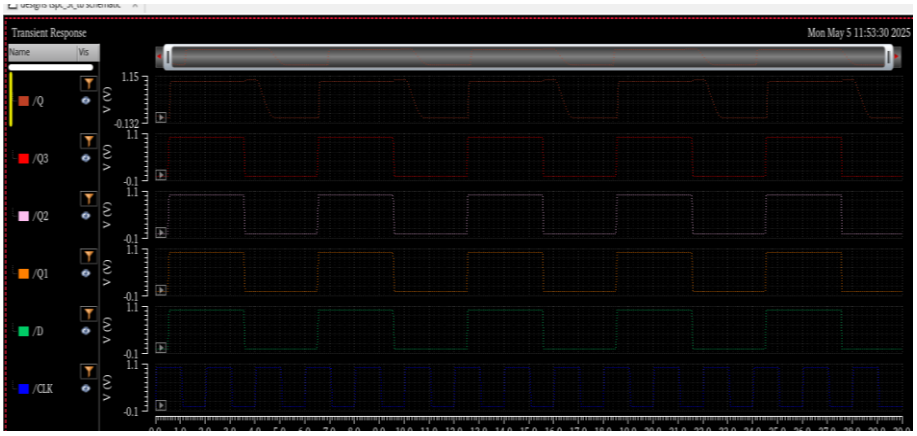

Fig.11: Transient Simulation of SISO Shift Register

Observations and Discussion

- The shift register performs accurate serial data shifting synchronized to the clock.
- TSPC D flip-flops show **no race-through or hold-time violations**, due to their dynamic logic structure and single-phase clocking.
- The power consumption is minimal due to reduced clock loading and transistor count.
- The design is compact, enabling integration into larger digital systems or as part of a data pipeline.

Power Consumption

This Table 1summarizes the dynamic power consumption of the SISO Shift Register during transient simulation. Power is measured based on supply voltage and switching activity of TSPC flip-flops.

1) Table 1: Power Consumption

Component	Supply Voltage (V)	Typical Power Consumption	Analysis Type
TSPC SISO Shift Register (4-bit)	1.2V	2.133 µW	Transient
Conventional D Flip Flop	1.2V	3.820 µW	Transient

The power consumption is measured under transient analysis using a supply of 1.2V.

V. CONCLUSION

This work demonstrates the design and simulation of a TSPC D Flip-Flop achieves lower power (2.133 µW) and reduced propagation delay (24.41 ps) compared to conventional designs. A 56% reduction in power and 70% improvement in speed are observed.

Its integration in a SISO shift register validates its suitability for sequential logic in high-performance VLSI. The design provides a compact, efficient solution for modern digital systems.

The future scope of the work are, the developed SISO shift register unit can be be integrated in the processor and SoCs (System on Chips), also the developed unit can be used in the cell development of ASIC(Application Specific Integrated Circuits).

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